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Strong Temperature Effect on the Ferroelectric Properties of $CuInP_2S_6$ and Its Heterostructures

Zijing Zhao, Kai Xu, Hojoon Ryu, and Wenjuan Zhu*

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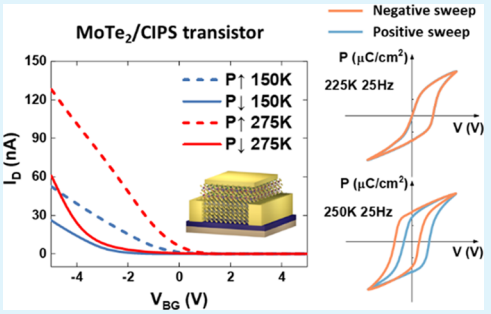
ABSTRACT: Van der Waals (vdW) ferroelectric insulator $CuInP_2S_6$ (CIPS) has attracted intense research interest due to its unique ferroelectric and piezoelectric properties. In this paper, we systematically investigate the temperature and frequency dependence of the ferroelectric properties of CIPS. We find that there is a large imprint in the CIPS capacitor, which can be attributed to the fixed dipoles induced by defects. At high temperatures and low frequencies, the amplitude and direction of the imprint become tunable by the preset pulse, as the copper ions are more mobile and these dipoles become switchable. When the polarization in CIPS changes direction, the graphene/CIPS/graphene ferroelectric diode exhibits switchable resistance since the Fermi level in graphene is modulated by the polarization in CIPS. For CIPS/$MoTe_2$ dual-gate transistor, a temperature-dependent nonvolatile memory window is observed, which can be attributed to the interplay between ferroelectric polarization and interface traps. This research provides experimental groundwork for vdW ferroelectric materials, expands the understanding of ferroelectricity in CIPS, and opens up exciting opportunities for novel electronic devices based on vdW ferroelectric materials.



KEYWORDS: *$CuInP_2S_6$, van der Waals ferroelectrics, temperature effect, ferroelectric heterostructure, imprint*

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INTRODUCTION

Ferroelectric materials with switchable polarization have broad applications including nonvolatile memory, electromechanical systems, and sensors.[1−4] Most technologically important ferroelectrics are perovskite oxides such as $PbZr_xTi_{1-x}O_3$ (PZT), $BaTiO_3$ (BTO), which are typically grown on crystal substrate via epitaxy.[5−7] However, these perovskites suffer from the lattice match restriction, surface dangling bonds, and incompatibility with silicon.[8,9] Recently, it was discovered that several van der Waals (vdW) materials are ferroelectric as well,[8] such as $CuInP_2S_6$ (CIPS),[10,11] In_2Se_3,[12−14] SnS,[15] SnSe,[16] SnTe,[17] WTe_2,[18] $MoTe_2$,[19] and hybrid perovskite BA_2PbCl_4.[20] Due to the weak van der Waals forces between layers, ultrathin ferroelectric flakes can be conveniently obtained. It is intriguing that these materials retain ferroelectricity even down to atomic scale. More importantly, these materials can be stacked on other vdW materials and form vertical heterostructures and superlattices with high-quality interfaces, providing a versatile material platform for multifunctional and reconfigurable devices.[21−24]

$CuInP_2S_6$ (CIPS) has a wide band gap (2.9 eV) and a high Curie temperature (315 K), which are important traits as a gate dielectric to ensure low leakage current and room-temperature operation of the electronic device.[10,25−27] In contrast to traditional ferroelectric materials, CIPS shows high ionic conductivity above 231 K due to the highly mobile Cu ions.[28] The defects in CIPS play an important role in its ferroelectric properties. Sulfur vacancy can induce a defect state near the valence band and suppress the ferroelectricity.[29] The interstitial Cu ions in vdW gaps lead to pinned dipoles and the negative piezoelectric effect.[30,31] The movement of the Cu ion is slower than that of electrons and has a strong temperature dependence.[32] These unique properties of CIPS together with its layered structure make it an intriguing candidate for novel ferroelectric heterostructures.

In this work, we investigate the temperature-dependent ferroelectric response of CIPS, and its implications for capacitors, ferroelectric diodes, and transistors. The ferroelectric switching of CIPS is affected by the strong polarization field of the defect dipoles, leading to an imprint in the hysteresis loop and small remanent polarization at low temperatures. Moreover, variable write measurement reveals the characteristic time constant for the ion-assisted switching. The temperature dependence of polarization is also confirmed in the ferroelectric heterostructures, including graphene/CIPS/graphene diodes and CIPS/$MoTe_2$ transistors. Ferroelectric resistive switching and ferroelectric memory window

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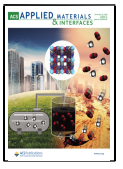

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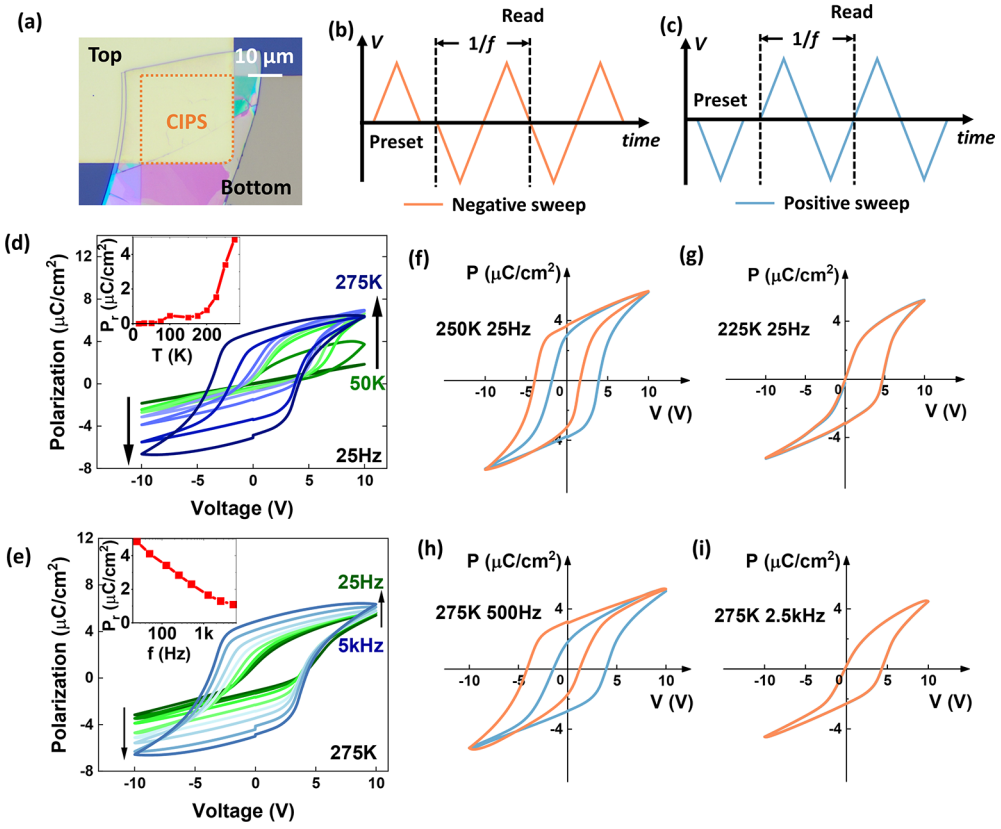

Figure 1. Temperature and frequency dependence of polarization in CIPS. (a) Optical image of a CIPS capacitor. The capacitance area is 627 μm^2. The CIPS thickness is 395 nm. (b, c) Pulse waveforms (voltage as a function of time) in the hysteresis loop measurements with negative and positive sweep directions respectively. (d) Temperature-dependent hysteresis loops measured at 25 Hz. The remanent polarization as a function of temperature is shown in the inset. (e) Frequency-dependent hysteresis loops measured at 275 K. The inset shows the remanent polarizations measured at various frequencies. (f–i) Imprint of the hysteresis at various temperatures and frequencies. (f) The hysteresis loops measured at 250 K using positive and negative sweeps shift to opposite directions. (g) The hysteresis loops measured at 225 K using positive and negative sweeps show identical imprint. Opposite shifts are also observed in 500 Hz sweep (h), while they are not observed in 2.5 kHz sweep (i) at 275 K.

were observed in these devices. These novel ferroelectric heterostructures offer new opportunities for both fundamental studies and applications in data storage and electronics.

RESULTS AND DISCUSSION

Ferroelectricity of CIPS was measured on metal/CIPS/metal capacitors. Figure 1a shows the optical image of a CIPS capacitor, where the active area is marked. The thickness of the CIPS is 395 nm. Triangular read pulses with a preset pulse are used to measure the hysteresis loops, and the different sweep directions are named as "positive" and "negative" according to the direction of the first read pulse (Figure 1b,c). The preset pulse has the same rise/fall time as the read pulses and has opposite polarity as the first read pulse. The periods of the pulses are longer than the RC delay of the measurement circuits. The temperature-dependent hysteresis loops of the capacitor measured using positive sweep are shown in Figure 1d. A symmetric hysteresis loop is observed at 275 K with a remanent polarization of 4.8 $\mu C/cm^2$, which is consistent with the previous reports on CIPS near room temperature.[10,26,27,33] When the temperature reduces from 250 to 100 K, the hysteresis loop shifts toward the positive direction, and the remanent polarization decreases, as shown in the inset of Figure 1d. No hysteresis loop is observed below 50 K. Figure 1e presents hysteresis loops measured at various frequencies at 275 K with the positive sweep. The low-frequency hysteresis loop is symmetric, while the hysteresis loops at high frequencies shift to the positive direction. The remanent polarization decreases logarithmically with the frequency, as shown in the inset of Figure 1e.

The imprint of the ferroelectric hysteresis loops can be attributed to the defect dipoles that cannot be switched at low temperatures or high frequencies. An opposite external electric field is required to cancel the polarization field from these dipoles; therefore, the central voltage of the hysteresis loop shifts oppositely. The Cu ions in CIPS are immobile when the temperature is below 231 K, and Cu atoms trapped in the interlayer sites can be the candidate for the pinned dipoles.[31,34] This hypothesis is supported by the hysteresis loops in Figure 1f–i measured with different sweep directions. At 250 K (Figure 1f), the hysteresis loop is shifted to the right under a positive sweep and to the left under a negative sweep. However, at 225 K (Figure 1g), identical right-shifted loops are observed for both sweep directions. This behavior is attributed to the temperature-dependent dipole switching. During the preset pulse, polarization of the dipoles can be aligned to the preset electric field, which causes the positive and negative shifts at 250 K. Since the dipole switching is associated with ion movement, these dipoles cannot switch at 225 K, which leads to identical hysteresis loops. The imprint of the ferroelectric hysteresis also has a strong frequency dependence. At 275 K, the imprint of the hysteresis loops measured at 500 Hz changes polarity depending on the sweep direction, as shown in Figure 1h. However, the imprint of the hysteresis

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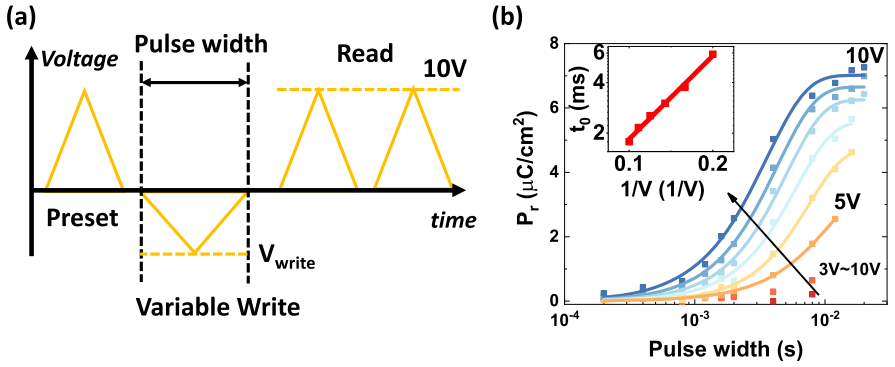

Figure 2. Variable write measurement and characteristic switching time in CIPS. (a) Illustrations of the pulse waveform used in the variable write measurement. The preset pulse pre-poles the film to certain polarization direction. The write pulse switches the polarization partially or completed depending on the amplitude and width of the pulse. The two read pulses measure the amount of polarization switched by the write pulse. (b) Switched polarization as a function of write pulse width at various pulse amplitudes. The inset shows the extracted characteristic switching time constant as a function of the reciprocal of the write pulse amplitude. The symbols are measured data, and the line is fitted using the NLS model.

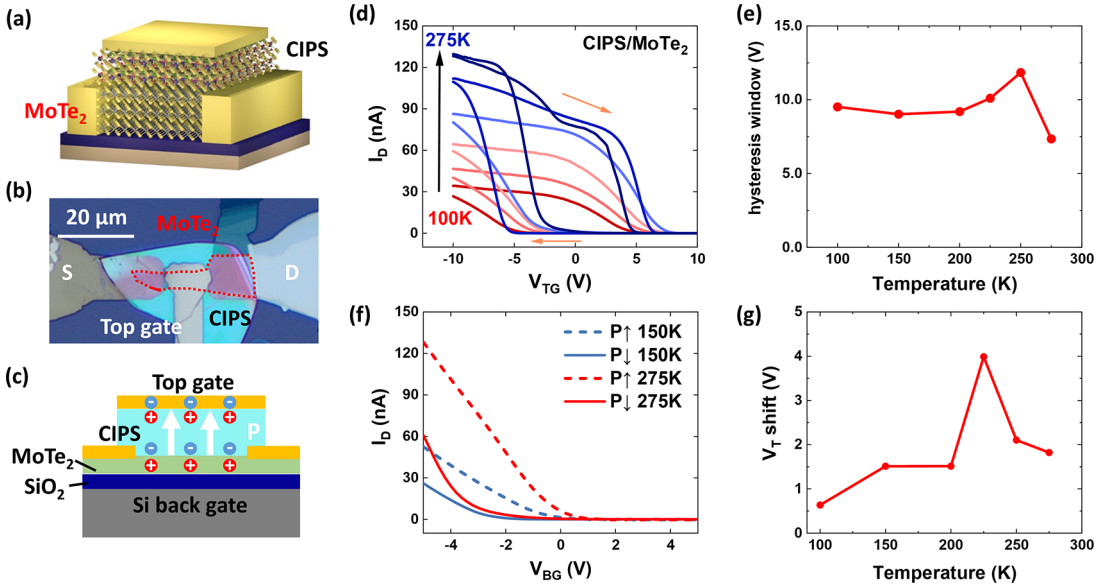

Figure 3. CIPS/$MoTe_2$ memory devices. (a, b) Schematic and optical image of a dual-gate $MoTe_2$ transistor with CIPS as the top-gate dielectric and 90 nm SiO_2 as the bottom-gate dielectric. The CIPS thickness is 310 nm, and the $MoTe_2$ thickness is 6.6 nm. Cr/Au and Ni/Au are used as channel contacts and top-gate electrode respectively. (c) Upward polarization in CIPS will induce hole doping in the $MoTe_2$ channel. (d) Transfer curves measured by sweeping the top gate at various temperatures. The clockwise hysteresis in the p-type transistor can be attributed to the ferroelectric switching. The drain voltage is 0.1 V. The temperature-dependent hysteresis window is shown in (e). (f) Memory effect measured using back gate. After applying positive or negative pulse on the top gate, the transfer curves are measured by sweeping the back gate. The transfer curve shifts to negative (positive) direction, corresponding to polarization down (up) states in the CIPS at both 150 and 275 K. (g) The memory window as a function of temperature.

loops at 2.5 kHz (Figure 1i) is identical regardless of the sweep direction, indicating that the defect dipoles are not switched by the fast preset pulse.

The switching behavior was further investigated using variable write measurement. The measurement consists of four voltage pulses, as illustrated in Figure 2a. The preset pulse pre-poles the film to certain polarization direction. The write pulse switches the polarization partially or completely depending on the amplitude and width of the pulse. The two read pulses measure the amount of polarization switched by the write pulse. The first read pulse is a switching pulse, while the second read pulse is a nonswitching pulse, which determines linear response of the dielectrics. By integrating the difference of the displacement currents in these two read pulses, we can extract the amount of polarization switched by the write pulse

$$P_{sw} = \frac{1}{A}\int_0^T (I_s - I_{ns})dt \quad (1)$$

where I_s and I_{ns} are the displacement currents measured in the first and second read pulses, respectively, A is the area of the device, and T is the pulse width. (The details of the variable write measurement are discussed in the Supporting Information.) The switched polarization measured at 275 K is plotted as a function of write pulse width at various pulse amplitudes, shown in Figure 2b. When the write pulse amplitude is low, one needs a rather long pulse to switch the polarization. In contrast, if the write pulse is sufficiently large, a short pulse

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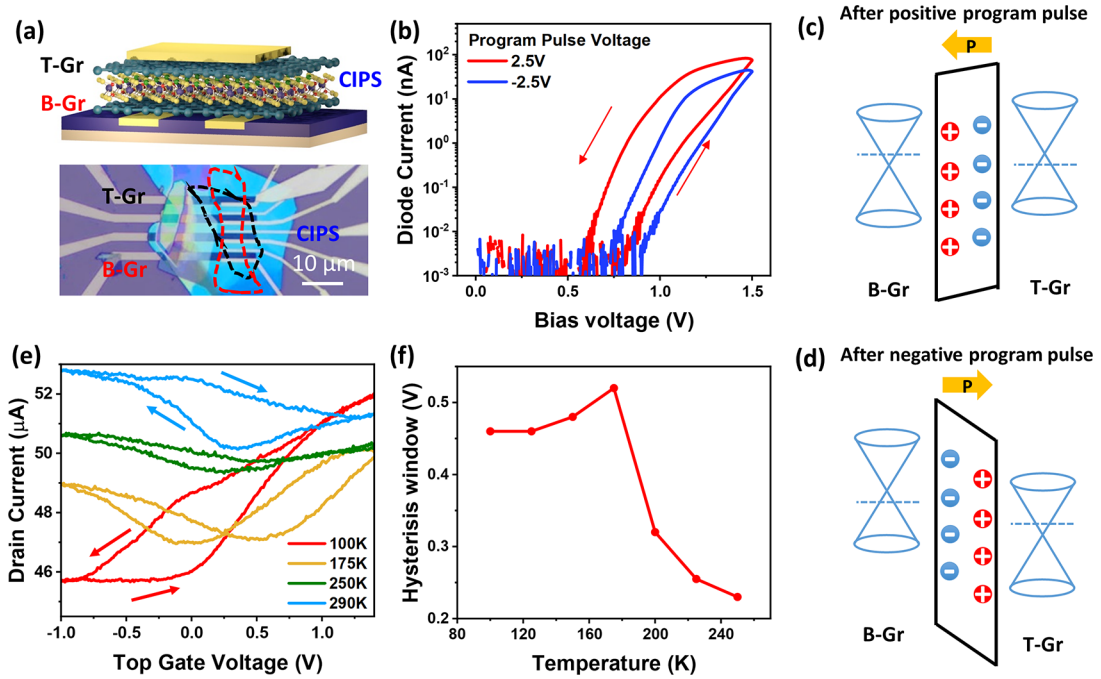

Figure 4. Graphene/CIPS multifunctional devices. (a) Schematic and optical image of a graphene/CIPS/graphene device. The thickness of the CIPS is 32 nm. (b) *IV* curves of graphene/CIPS/graphene ferroelectric vertical diode after positive and negative program pulses. The program pulse and DC drain voltage are applied on the top graphene with the bottom graphene grounded. (c, d) Band diagrams of graphene/CIPS/graphene after positive and negative program pulses, respectively. (e) Temperature-dependent transfer curves of the transistor with bottom graphene as channel, CIPS as the gate dielectric, and top graphene as gate. (f) Temperature-dependent hysteresis window of the graphene/CIPS transistor.

could switch a large amount of polarization. These results fit well with the nucleation-limited switching (NLS) model[35]

$$p(t) = 1 - e^{-(t/t_0)^n} \quad (2)$$

where $p(t)$ is the fraction of the volume of the ferroelectric switched by time t, t_0 is a characteristic switching time, and n is a parameter related to geometric dimension of the domain growth. The extracted n value shows a narrow distribution in the range of 1.4−1.6. The characteristic switching time is plotted as a function of $1/V$, where V is the applied voltage, as shown in the inset of Figure 2b. The data are fitted using Merz's law: $\tau = \tau_0 \exp((V_0/V)^n))$, where $n = 1$ is used here; τ_0 is the switching time at infinite applied electric field and V_0 is the activation voltage.[36] The extracted τ_0 in CIPS is 0.59 ms, which is several orders of magnitude longer than τ_0 in doped HfO_2 (0.1 ps),[37] indicating that the polarization switching in CIPS is very slow.

Based on the understanding of the ferroelectricity in CIPS, we further investigated the electronic devices based on CIPS heterostructures. First, we studied ferroelectric memory based on CIPS/$MoTe_2$ stacks. The structure and optical image of the device are shown in Figure 3a,b respectively. Dual-gate $MoTe_2$ transistors are fabricated, where CIPS serves as the top-gate dielectric and 90 nm SiO_2 serves as the bottom-gate dielectric. The CIPS thickness is 310 nm, and the $MoTe_2$ thickness is 6.6 nm. When the CIPS polarization switches direction, the polarization-induced doping in the $MoTe_2$ channel will also change polarity. A negative bias on the top gate will induce upward polarization, leading to hole doping to the $MoTe_2$ channel, as shown in Figure 3c. Conversely, a positive bias will introduce electron doping in $MoTe_2$. The transfer curve measured by sweeping the top gate shows a clockwise hysteresis loop for all temperatures (Figure 3d), which can be attributed to the ferroelectric switching at these temperatures. Further, the hysteresis window, defined as the shift of threshold voltage between the forward and backward sweeps, is plotted as a function of temperature, as shown in Figure 3e. As the temperature increases from 150 to 250 K, the hysteresis window increases slightly, indicating more dipoles become switchable. When the temperature exceeds 250 K, the hysteresis window starts to decrease and the underlying mechanism can be 2-fold. First, the interface traps at the $MoTe_2$/CIPS interface are more active at high temperatures. Since the hysteresis induced by the interface traps is in the opposite direction to that induced by ferroelectric polarization, the total hysteresis window will reduce as temperature increases. Second, the dielectric constant of CIPS also increases as the temperature approaches the Curie temperature, which will lead to a smaller threshold voltage shift for a given polarization charge density.[38] The memory effect is also studied using back gate. Here, a square pulse with pulse amplitude of 8 V and pulse width of 10 s is applied on the top gate to pole the CIPS into upward or downward polarization. Furthermore, the memory windows of the CIPS/$MoTe_2$ transistors were also investigated. After applying positive and negative program pulses on the top gate, the transfer curves were measured by sweeping the back-gate bias, as shown in Figure 3f. A negative program pulse on the top gate will switch the polarization in CIPS to an upward direction, which will induce hole doping in the $MoTe_2$ channel and a positive shift in the threshold voltage. The memory window, defined as the difference between the threshold voltages after positive and negative program pulses, is plotted as a function of temperature, as shown in Figure 3g. The memory window is found to increase from 100 to 225 K due to increased

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remanent polarization in CIPS. The decrement of the memory window after 225 K indicates that the interface traps at the $SiO_2/MoTe_2$ interface start to shift the threshold voltage in an opposite direction.

Furthermore, we investigated the multifunctional devices based on graphene/CIPS/graphene heterostructures. The schematic and optical image of the device are shown in Figure 4a. CIPS is sandwiched by two layers of graphene in the vertical direction. In each layer of graphene, there are multiple electrodes so that both the vertical and lateral transport can be characterized concurrently. This device can serve as a ferroelectric junction, memory device, and logic device simultaneously. First, we investigated the ferroelectric junction between top and bottom graphene electrodes. A program pulse was applied on the top graphene electrode with bottom graphene electrode grounded. Then, the current of the junction was measured by sweeping the voltage on the top graphene, as shown in Figure 4b. We can see that the *IV* curve of the junction shifts toward the negative direction after positive program pulse. The current shift can be attributed to the polarization switching in CIPS. Figure 4c,d displays the energy diagrams of graphene/CIPS/graphene heterostructure after positive and negative program pulses, respectively. After positive program pulse, a downward polarization is formed in CIPS, which will induce negative charges and raise the Fermi level in the bottom graphene. The reduced Schottky barrier between the bottom graphene and CIPS will lead to a higher electron current, which is consistent with the left shift of the *IV* curve observed experimentally. Second, we studied the CIPS/graphene ferroelectric transistor, where the top graphene serves as the gate, the bottom graphene serves as the channel, and CIPS serves as the gate dielectric. Figure 4e shows the temperature-dependent transfer curves of the graphene transistor measured from 100 to 290 K. All curves exhibit clockwise hysteresis loops for hole branch and counterclockwise hysteresis loops for electron branch, which are typical features for ferroelectric transistor. More importantly, the CIPS/graphene transistor exhibits no obvious ferroelectric hysteresis below 50 K, which is consistent with the temperature dependence of polarization in the CIPS capacitors, as shown in the inset of Figure 1d. Further, the hysteresis window of the graphene transistor is plotted as a function of temperature, shown in Figure 4f. As the temperature increases, the hysteresis window first increases and then decreases, similar to the $CIPS/MoTe_2$ transistor, which can be explained by the temperature dependence of polarization in CIPS and the influence of interface traps at high temperatures.

CONCLUSIONS

In summary, the temperature and frequency dependences of remanent polarization in CIPS capacitor are investigated systematically. The remanent polarization decreases dramatically as temperature goes below 250 K and disappears as temperature decreases below 50 K. Moreover, the remanent polarization degrades logarithmically as frequency increases. These phenomena can be explained by the defect-related dipoles, which pin the polarization at low temperatures and become switchable at high temperatures. These defect dipoles also lead to the strong temperature and frequency dependence of the imprint of the CIPS capacitors. These unique characteristics of CIPS are important factors to consider in designing and characterizing CIPS-based electronic devices. Based on the understanding of the ferroelectricity in CIPS, we further investigated the electronic devices based on CIPS heterostructures including $CIPS/MoTe_2$ memory and graphene/CIPS/graphene multifunctional devices. Memory window and ferroelectric-induced resistive switching are observed in these devices, which can be explained by the electrostatic doping induced by the ferroelectric polarization. Temperature dependence of the hysteresis window in the CIPS transistors can be attributed to the interplay between remanent polarization in CIPS and interface traps. This research enriches the understanding of van der Waals ferroelectric materials and opens new opportunities for multifunction devices based on two-dimensional (2D) ferroelectric heterostructures.

METHODS

The CIPS capacitors were fabricated on highly doped Si substrate with 90 nm SiO_2. The bottom electrodes were patterned using photolithography followed by metal deposition of 5/15 nm Cr/Au. CIPS flakes were exfoliated on poly(dimethylsiloxane) (PDMS) films and then transferred onto the bottom electrodes. The top electrodes (20/50 nm Ni/Au) were then formed on CIPS. For the dual-gate memory devices, the $MoTe_2$ channels were exfoliated on p-type Si substrate with 90 nm SiO_2. Cr/Au (5/15 nm) was deposited to serve as the S/D contact. The CIPS flakes were then transferred on top of the $MoTe_2$ channel. A subsequent photolithography step defined the top gates, and 20/80 nm Ni/Au was used as the top electrode. For the graphene/CIPS multifunctional devices, the CIPS flakes were exfoliated on the transparent gel film. Bulk graphite was exfoliated on a poly(methyl methacrylate)/poly(vinyl alcohol) (PMMA/PVA) film, and monolayer graphene can be identified by optical microscopy. Then, graphene, CIPS, and graphene are transferred on the bottom electrode (5/10 nm Ti/Au) respectively. Finally, electron beam lithography, metal deposition (5/20 nm Ti/Au), and liftoff process were conducted sequentially. We have fabricated four CIPS capacitors, three $CIPS/MoTe_2$ transistors, and two CIPS/graphene transistors. The representative results are shown in the main text and in the Supporting Information.

The voltage pulses were generated by Keithley 4225-RPM units, and the current was collected using a Keithley 4200-SCS analyzer. A Keysight B1500A analyzer was used to characterize CIPS memory devices and graphene/CIPS/graphene heterostructures. The thicknesses of the CIPS and $MoTe_2$ flakes were measured using an Asylum Cypher atomic force microscope (AFM).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.0c13799.

Procedure of variable write measurement for extraction of switchable polarization in CIPS; AFM topographic images and height profiles of the CIPS devices; comparison of the drain current and gate current of the CIPS transistors; and temperature-dependent transfer curves of the CIPS/graphene transistor (PDF)

AUTHOR INFORMATION

Corresponding Author

Wenjuan Zhu − *Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, United States;* orcid.org/0000-0003-2824-1386; Email: wjzhu@illinois.edu

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Authors

Zijing Zhao − *Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, United States*

Kai Xu − *Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, United States*

Hojoon Ryu − *Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.0c13799

Author Contributions

Z.Z. and K.X. contributed equally. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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