TOPICAL REVIEW

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Abstract

Two-dimensional (2D) transition metal dichalcogenides (TMDs) have very versatile chemical, electrical and optical properties. In particular, they exhibit rich and highly tunable electronic properties, with a bandgap that spans from semi-metallic up to 2 eV depending on the crystal phase, material composition, number of layers and even external stimulus. This paper provides an overview of the electronic devices and circuits based on 2D TMDs, such as Esaki diodes, resonant tunneling diodes (RTDs), logic and RF transistors, tunneling field-effect transistors (TFETs), static random access memories (SRAMs), dynamic RAM (DRAMs), flash memory, ferroelectric memories, resistitive memories and phase-change memories. We address the basic device principles, the advantages and limitations of these 2D electronic devices, and our perspectives on future developments.

1. Introduction

TMDs have a general formula of MX_2, where M is a transition metal atom (such as Ti, Zr, Hf, V, Nb, Ta, Re, etc) and X is a chalcogen atom (such as S, Se, Te). There are over 30 different TMDs with diverse properties, ranging from semiconductors (MoS_2, WSe_2) to semimetals (1T′ phase WTe_2 and $TiSe_2$), metals (VSe_2, NbS_2), and superconductors ($PbTe_2$, $NbSe_2$) [1–16]. Monolayer TMDs have four polymorphs: 1H phase (space group $P\bar{6}m2$), 1T phase (space group $P\bar{3}m2$), 1T′ phase (space group $P2_1/m$), and $1T_d$ phase (space group $P1m1$) [17–23]. When the TMDs are stacked together, they can form three types of structural polytypes: 2H (hexagonal symmetry, two layers per repeat unit, trigonal prismatic coordination), 3R (rhombohedral symmetry, three layers per repeat unit, trigonal prismatic coordination) and 1T (tetragonal symmetry, one layer per repeat unit, octahedral coordination) [24]. Most of the bulk TMDs (such as WS_2 and $MoTe_2$) are stable in 2H phase and exhibit semiconductor behavior, while some of the TMDs (such as WTe_2) are stable in the 1T phase and exhibit metallic behavior at room temperature [25]. These diverse crystal structures and material properties make TMDs attractive candidates for a large variety of electronic and photonic applications. In addition, unlike graphene, TMDs can be synthesized on insulating substrates in large scale, which is another important factor that drives intense research and development interest in TMDs. The common synthesis methods for TMDs include chemical vapor deposition (CVD) [26–36], physical vapour deposition (PVD) [37, 38], metal-organic CVD (MOCVD) [39, 40], metal transformation [41], chemical vapor transport (CVT) [42, 43], chemical or electrochemical exfoliation [44–46], pulsed laser deposition (PLD) [47], molecular beam epitaxy (MBE), spray pyrolysis [48], and atomic layer deposition (ALD) [49, 50]. Among these methods, CVD and MOCVD are the most widely investigated methods and wafer-scale TMDs have been demonstrated using MOCVD [39]. The band structure, synthesis, material properties, and applications of various 2D materials including graphene, transition metal dichalcogenide and black phosphorus have been reviewed in several articles [1, 4, 24, 32, 50–57]. In this paper, we focus on the electronic devices based on TMD materials and provide

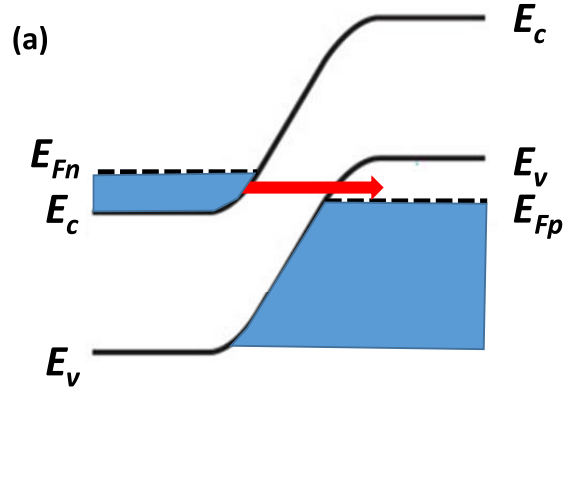

Figure 1. Illustration of (a) energy band diagram and (b) *IV* characteristics of an Esaki diode.

comprehensive overview of the operating principles, the state-of-the-art, the potential and the challenges of TMD based electronic devices.

2. Electronic devices based on TMDs

2.1. Two-terminal devices

Esaki diodes and RTDs are two-terminal devices with prominent negative differential resistance (NDR). An Esaki diode is based on interband tunneling, while an RTD is based on intraband tunneling.

2.1.1. Esaki diodes

The band diagram and typical IV characteristics of the traditional Esaki diode are shown in figures 1(a) and (b) [58]. In the forward bias, electrons flow from the filled states in the conduction band in the n-type semiconductor to empty states in the valence band in the p-type semiconductor. As the forward bias is increased, the conduction band of the n-type semiconductor is eventually raised above the valence band of the p-type semiconductor, electrons can no longer tunnel into a valence-band state while conserving both total energy and transverse momentum, and the current is reduced to a minimum. Further increasing the bias will increase the current due to the thermionic emission over the energy barrier.

Various material stacks have been used in Esaki diodes, including Si, Ge, SiGe, III–V, and their heterostructures [59–65]. Peak current density up to 2.2 MA cm^{-2} has been demonstrated in Esaki diodes based on InAs/GaSb heterojunctions [61]. Excellent average peak-to-valley current ratio (PVR) of 14 was achieved in Esaki diodes based on n-$In_{0.5}Ga_{0.5}As$/p-$GaAs_{0.5}Sb_{0.5}$ [66]. Recently, 2D crystals have emerged as promising candidates for Esaki diodes. 2D materials are free of surface dangling bonds, and 2D heterostructures mediated by van der Waals (vdW) forces are free of dislocations even when there is a large mismatch in their lattice constants. The ability to stack heterostructures without the constraint of lattice matching opens up tremendous opportunities in the engineering of various band alignments for tunneling devices, down to the atomic level. Yan *et al* demonstrated Esaki diodes based on the vdW heterostructure of black phosphorus (BP) and tin diselenide ($SnSe_2$), shown in figures 2(a) and (b) [67]. These two semiconductors form a type III or broken-gap energy band alignment. The presence of an vdW gap, which serves as a thin insulating barrier between BP and $SnSe_2$, enables the observation of a prominent NDR region in the forward-bias region. PVR of 1.8 at 300 K and peak current density ~1.6 kA m^{-2} were observed [67]. Esaki diode based on vertical heterostructure of MoS_2 and WSe_2 also shows NDR at low temperatures (figures 2(c) and (d)) [68]. Shim *et al* demonstrated an Esaki diode based on a phosphorene/rhenium disulfide (BP/ReS_2) heterojunction. The PVR ratio of these devices can reach 4.2 at room temperature. Utilizing these diodes, the authors developed multi-valued logic circuits [69]. Recently, Esaki diodes based on 2D/3D heterojunctions also have been explored. Xu *et al* demonstrated Esaki diodes based on MoS_2 on degenerately-doped silicon, while Krishnamoorthy *et al* demonstrated Esaki diodes based on MoS_2 on GaN [70, 71]. The PVR ratios of these 2D/3D Esaki diodes are ~1.2 [69–71]. Further material and process optimizations are still needed for the 2D TMD based Esaki diodes to be competitive with the III–V based Esaki diodes. However, the ability to freely stack the 2D layers and manipulate their orientation angle allows for greater degree of band alignment control, an attractive attribute for tunneling based devices.

2.1.2. Resonant tunneling diodes (RTDs)

The band diagram and typical IV characteristics of a traditional RTD are illustrated in figures 3(a) and (b) [58]. The RTD consists of a double potential barrier. The quasi-Fermi levels in the left contact, E_F, and right contact, E_F—eV, are split by the applied voltage V. The horizontal line between the barriers represents the

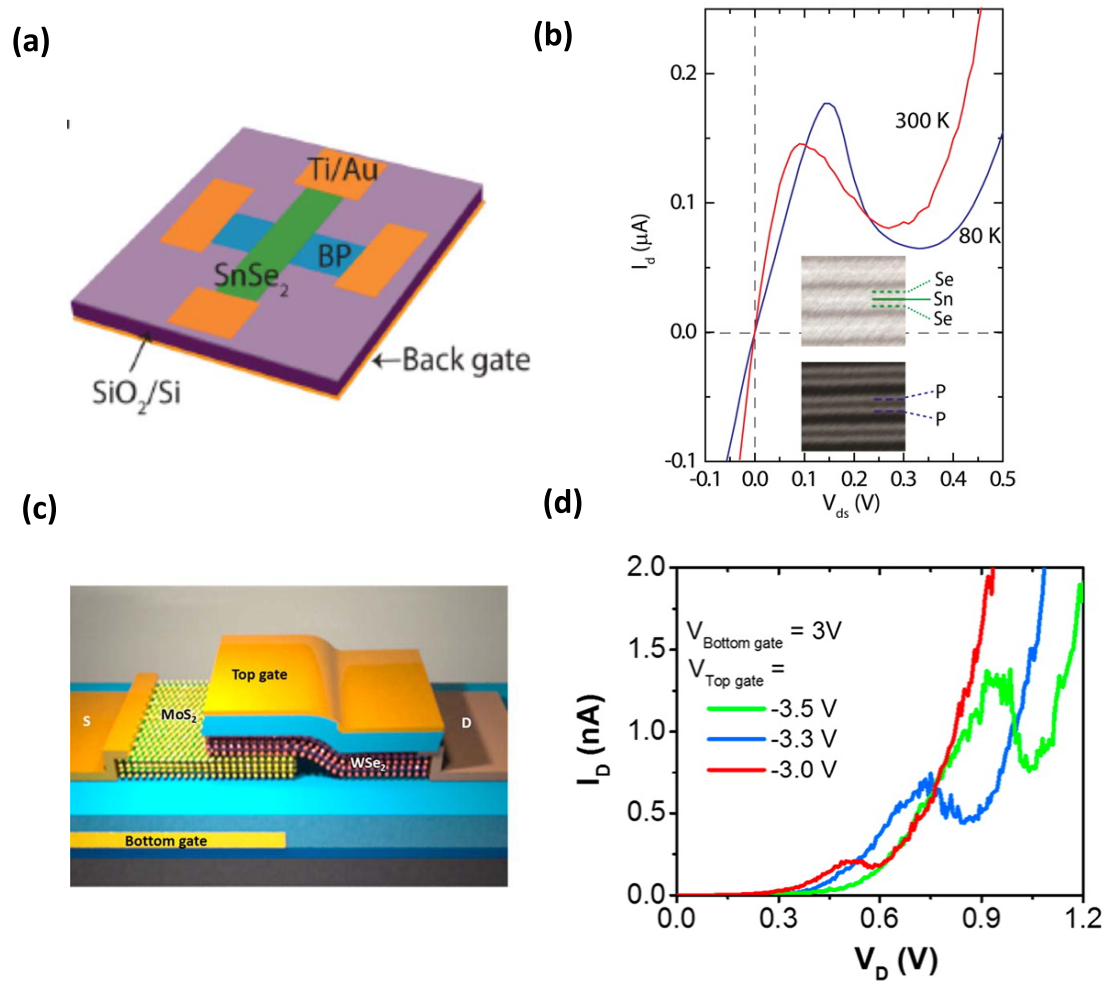

Figure 2. Esaki diodes based on 2D TMDs. (a) and (b) Structure and current–voltage characteristics of the BP/$SnSe_2$ vdW Esaki diode [67]. (c) and (d) Three-dimensional schematic and $I_D V_D$ of an Esaki diode based on a vertical heterostructure of MoS_2 and WSe_2 [68].

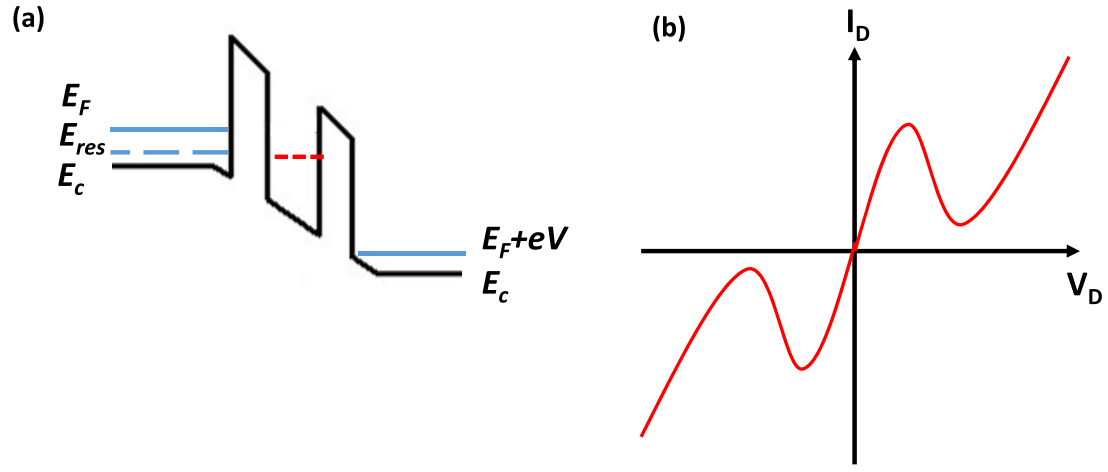

Figure 3. Illustration of (a) energy band diagram and (b) *IV* characteristics of an RTD.

energy of the resonant state of the semiconductor in the quantum well. As bias is applied on the right contact, the resonant level is pulled down to the Fermi level of the emitter on the left. At this point, when $E_{res} = E_F$, the current turns on. As the bias is increased, the resonant level is pulled deeper into the Fermi sea of the emitter and the current increases with bias. Once the resonant energy falls below the conduction band of the emitter,

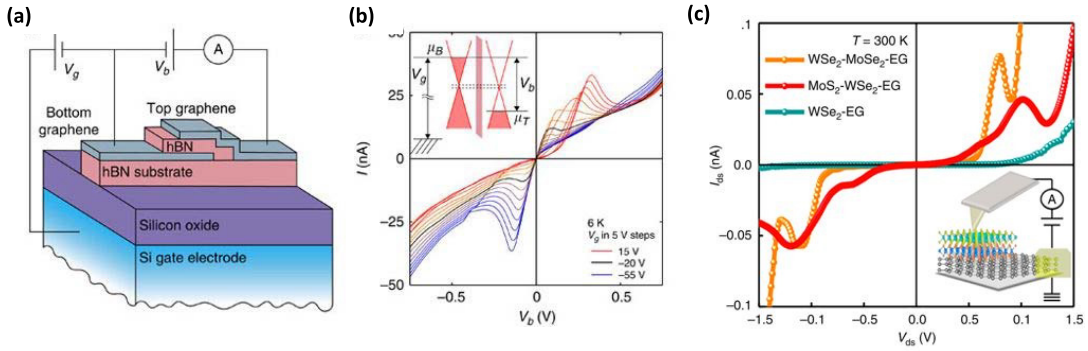

Figure 4. RTDs based on 2D materials. (a) and (b) Schematic diagram and measured current–voltage characteristics of a graphene-BN RTD [72]. (c) Experimental *I*–*V* traces for different combinations of dichalcogenide-graphene interfaces [76].

electrons can no longer tunnel while conserving both total energy and transverse momentum, and the current reaches a minimum.

Vertical stacking of 2D materials can form a double potential barrier naturally without any lattice matching restriction. It was observed experimentally that resonant tunneling can occur when the energy bands of two 2D semiconductors separated by a tunneling barrier are aligned. Britnell *et al* reported resonant tunneling of Dirac fermions in two graphene layers through a boron nitride barrier, shown in figures 4(a) and (b). The resulting NDR in the device characteristics persists up to room temperature and is gate-voltage tunable. Since the carriers tunnel across only a few atomic layers, these devices have the potential of ultrafast transit times [72]. Zhao *et al* simulated a symmetric tunneling field-effect transistor (SymFET) which consists of an n-type graphene layer and a p-type graphene layer. The authors found that a large current peak occurs when the Dirac points of the two graphene layers are aligned at a particular drain-to-source bias and the resonant current peak is controlled by chemical doping and applied gate bias [73]. NDR has also been observed in rotationally aligned double bilayer graphene heterostructures separated by hexagonal boron nitride (hBN) dielectric [74, 75]. In addition, NDR effects exist in TMD heterostructures as well. Lin *et al* demonstrated direct synthesis of atomically thin TMDs on graphene [76]. The conductive atomic force microscopy (CAFM) measurements on MoS_2–WSe_2-graphene and WSe_2–MoS_2-graphene heterostructures show resonant tunneling and room-temperature NDR characteristics, shown in figure 4(c). The NDR and fast response time in Esaki didoes and RTDs make them promising in applications including oscillators, THz detectors, multi-value memories, and analog-to-digital converters. However, a key challenge in making these vertical heterostructure based devices is the stringent requirement on matching the momentum space between layers; otherwise, transport across the layers would be phonon-mediated and would tend to degrade the performance [77].

2.2. Transistors

2.2.1. Logic transistors

Traditional logic transistors based on silicon are facing severe challenges in device scaling. A common approach used to suppress short-channel effect involves reducing the channel thickness to enhance the gate electrostatic control on the channel. In the past, silicon-on-insulator (SOI), ultra-thin SOI (UTSOI) and extremely thin SOI (ETSOI) have been pursued [78, 79]. However, the mobility degrades and threshold voltage varies significantly as the thickness is scaled down due to surface roughness [80–83]. TMDs with atomically thin body and sizable bandgap can uniquely address these challenges [55, 84]. Simulations revealed that monolayer MoS_2 FETs show 52% smaller drain-induced barrier lowering (DIBL) and 13% smaller subthreshold swing (SS) than 3 nm thick-body Si FETs at a channel length of 10 nm [85]. Figure 5(a) shows that monolayer MoS_2 with double gate can effectively reduce DIBL as compared to silicon SOI technology [86]. In the meantime, 2D materials suffer much less mobility degradation as compared to silicon, when the channel thickness reduces to nanometer scale, shown in figure 5(b). Cao's simulation indicated that MoS_2 FETs can meet high performance (HP) requirement up to 6.6 nm gate length using bilayer MoS_2 as the channel material. The scaling of the TMD transistors was also explored experimentally [87–89]. Yang *et al* demonstrated scaled devices with 10 nm channel length as well as ultrathin (2.5 nm) gate dielectrics which show effective immunity to short-channel effects, shown in figure 5(c) [90]. Desai *et al* demonstrated MoS_2 transistors with a 1 nm physical gate length using a single-walled carbon nanotube (SWCNT) as the gate electrode, illustrated in figure 5(d). These ultra-short devices show near ideal subthreshold swing of ~65 mV per decade and high On/Off current ratio of ~10^6 [91]. These results clearly show that TMDs have high potential in extremely scaled logic devices.

Due to the atomically thin bodies and large bandgaps of TMD materials, the contact resistances in

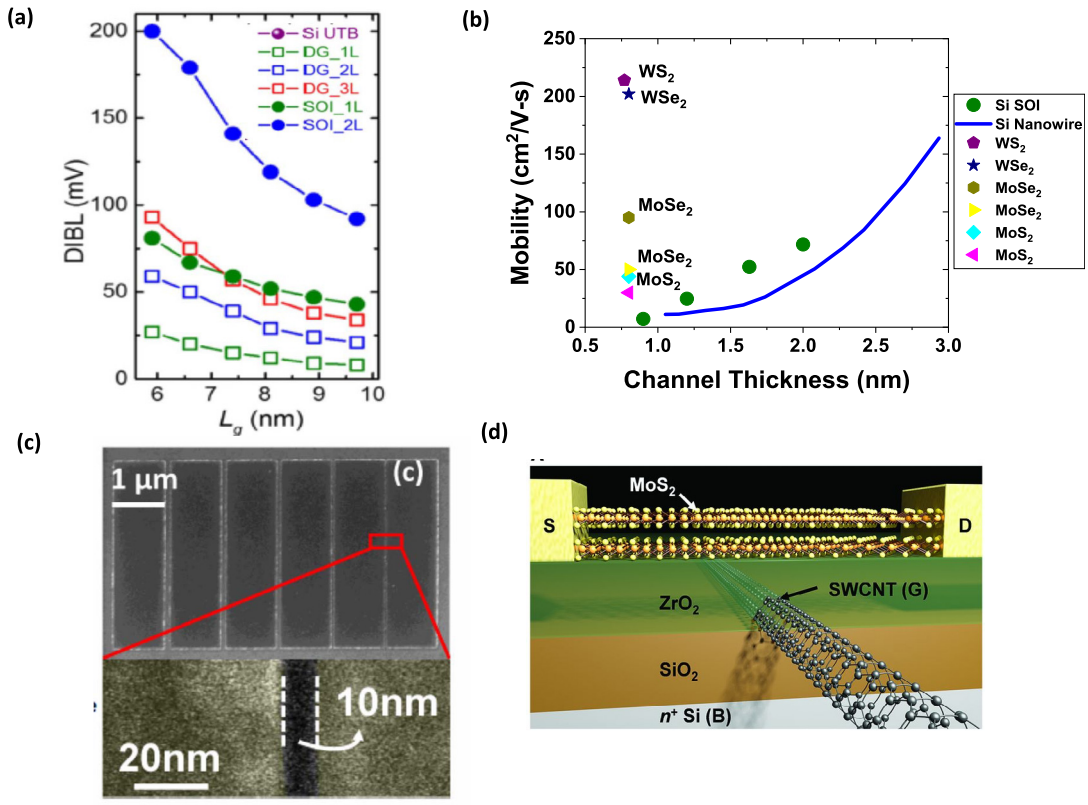

Figure 5. Scaling of TMD logic transistors. (a) Drain-induced barrier lowering (DIBL) with gate length scaling for 1L–3L MoS_2 FETs and Si ultra-thin-body (UTB) transistor. SOI and DG stand for semiconductor-on-insulator and double-gate, respectively [86]. (b) Carrier mobility as a function of channel thickness. Data for WS_2, WSe_2, $MoSe_2$ and MoS_2 are taken from [31, 39, 171–175]. Data for silicon SOI and silicon nanowire are taken from [176, 177]. (c) SEM image of the MoS_2 transistors with 10, 20, 40, 60, and 80 nm nominal channel length after the deposition of 40 nm Ni. Magnified part shows the 10 nm nominal channel length [90]. (d) Schematic of 1D2D-FET with a MoS_2 channel and SWCNT gate [91].

TMD transistors are usually much higher than those in transistors based on graphene and black phosphorus [92]. Reducing contact resistance in TMD transistors is one of the key issues that needs to be addressed before 2D TMD based electronic and photonic devices can be competitive with the current state-of-the-art electronic devices. Several approaches have been investigated to reduce contact resistance [93], including using low work-function metals for n-channel FETs (high work function for p-channel FETs) [94, 95], increasing doping in the source/drain region [96–98], converting semiconducting 2H phase to metallic 1T phase at the contact region [99], or using graphene as contact to resolve the Fermi-level pinning issues and tune the work function electrically [100–103].

The performance of the TMD transistors is also influenced by the defects in the TMD layers, the charge impurities and the topography of the gate dielectrics and the substrates [104–107]. Zhu *et al* quantified the density of the gap states in CVD MoS_2 on SiO_2 substrate and found that the trapped charges can degrade subthreshold slope, and also lead to a large underestimation of the true band mobility [88]. Cui *et al* showed that encapsulating MoS_2 layers with hexagonal boron nitride, in conjunction with the utilization of edge contact, can significantly reduce the extrinsic scattering and demonstrated Hall mobility of 34 000 $cm^2 V^{-1} s^{-1}$ for six-layer MoS_2 at low temperature (~3 K) [103].

2.2.2. RF transistors

Traditional RF devices were typically based on silicon, SiGe and III–V materials. The maximum frequency of oscillation, f_{max}, based on III–V materials has exceeded 1 THz [108]. To further increase the operating frequency and bandwidth, higher mobility and saturation velocity material and further optimized device structures/processes with less geometric and parasitic capcitance are needed. Graphene was intensely investigated as a potential candidate for RF devices, due to its extremly high carrier mobility. The cut-off frequency, f_T, of graphene RF devices was shown to be comparable to that of the best available III–V RF devices [109–113]. However, since graphene does not have a bandgap, it is very difficult to achieve current saturation, which will limit the f_{max} and power gain of the RF devices. TMDs with sizable bandgap can potentially address this issue. Krasnozhon *et al* demonstrated top-gated MoS_2 RF transistors with f_T reaching 6 GHz and f_{max} of 8.2 GHz on silicon substrate, illustrated in figure 6(a) [114]. Cheng *et al* demonstrated a high-performance MoS_2 RF device on flexible substrate with an intrinsic cut-off frequency f_T

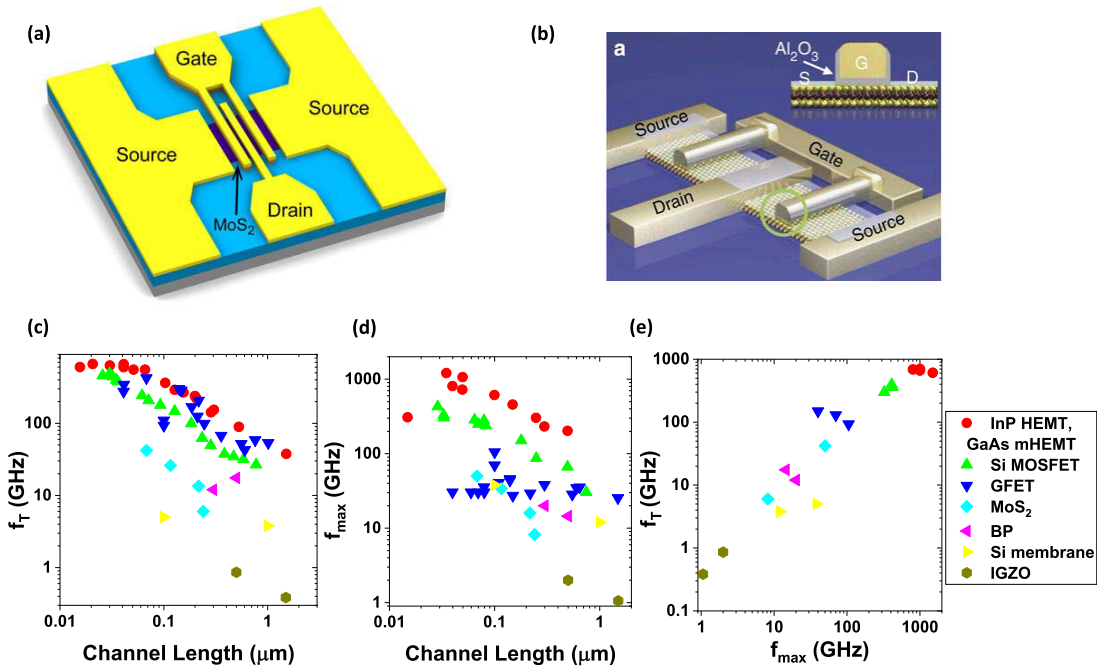

Figure 6. RF transistors based on TMDs. (a) An illustration of a MoS_2 RF device with metal gate. (b) A schematic illustration of a dual-channel self-aligned MoS_2 FET with transferred gate stacks, and the inset shows the schematic cross-section of the self-aligned device. (c) Cut-off frequency f_T and (d) maximum oscillation frequency f_{max} as a function of gate length of MoS_2 RF transistors, together with the representative results for RF devices based on graphene, black phosphorus (BP), InP, GaAs, Si, IGZO and silicon nanomembranes. (e) f_T versus f_{max} of MoS_2 RF transistors, together with the best results reported for RF devices based on graphene, BP, InP, GaAs, Si, IGZO and silicon nanomembranes. For (c)–(e), data for MoS_2 RF transistor are taken from [114, 115]. Data for black phosphorus are taken from [178, 179]. Data for graphene is taken from [111, 180–182]. Data for SI MOSFET, InP HEMT and GaAs HEMTs are taken from [182, 183]. Data for silicon nanomebranes are taken from [184, 185]. Data for IGZO are taken from [186, 187].

up to 42 GHz and a maximum oscillation frequency f_{max} up to 50 GHz, and an intrinsic gain over 30, shown in figure 6(b) [115]. Figures 5(c) and (d) show f_T and f_{max} of TMD RF devices, together with the best RF devices based on graphene, black phosphorus, silicon, III–V materials, silicon nanomembranes and indium gallium zinc oxide (IGZO). For flexible electronics, the RF devices based on TMDs are very promising, as the f_T and f_{max} of the TMD RF devices are higher than or comparable to that of RF devices based on other flexible electronic materials such as silicon membrane and IGZO. For electronics on rigid substrates, however, RF devices based on III–V materials and silicon are more promising, since TMDs have limited mobilities and high contact resistances. The issue of limited mobilities should become less important as device channel length approaches that of the scattering mean free path, and entering the ballistic transport limit. Achieving low Ohmic contact resistance presents a more pressing issue in this regard.

2.2.3. Tunneling field-effect transistors (TFETs)

Power consumption is one of the main challenges for future electronics. Reducing the subthreshold swing is key to lowering the supply voltage and power consumption. In a conventional MOSFET, the minimum subthreshold swing (SS) is 60 mV/decade at room temperature, determined by the thermal energy of the carriers. This places a fundamental limit on the supply voltage. TFET can overcome this limit by using band-to-band tunneling, rather than thermal injection, to inject charge carriers into the device channel [116–118]. In TFETs, the carriers in the source are energetically forbidden to tunnel to the channel in the OFF state, due to the lack of available states in the channel, illustrated in figure 7(c). This effectively cuts off the current induced by the carriers in the high-energy tail of the Femi–Dirac distribution. When the device is turned on, i.e. the conduction band of the channel is below the valence band edge of the source region, the electrons can now tunnel from the source to the channel, as illustrated in figure 7(d). This ON/OFF switch is controlled by the availability of the energy states in the channel, instead of the carrier energy distribution, resulting in a much steeper subthreshold swing in TFET as compared to MOSFET.

Researchers have explored various TFET devices using group IV semiconductors [119, 120], III–V semiconductors [121], and carbon based materials [122]. InAs/silicon heterostructure TFETs show sub-threshold swing as low as 20 mV/decade; however, the on-current is only ~6 nA μm^{-1} [123, 124]. Type II arsenide/antimonide compound semiconductor with highly staggered $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterojunction demonstrated very high on-current (190 $\mu A\ \mu m^{-1}$ at $V_{DS} = 0.75$ V); however, the subthreshold

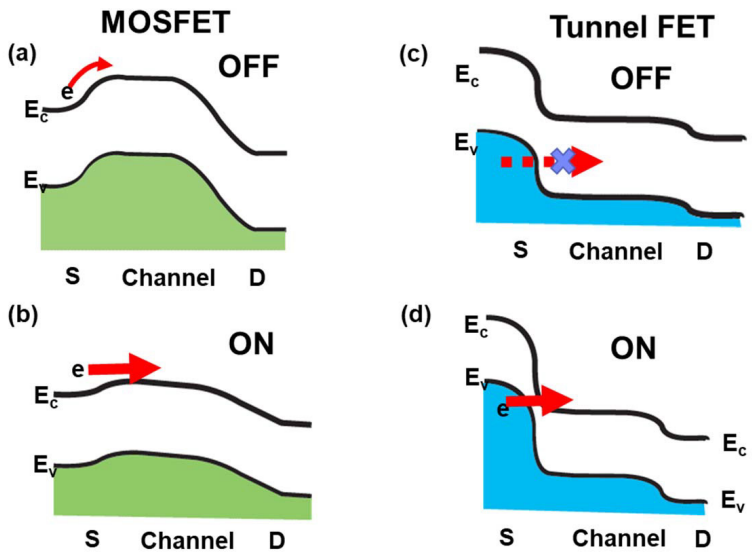

Figure 7. Energy diagram of MOSFET and TFETs. Figures (a) and (b) are the energy diagrams of a MOSFET at OFF and ON states. Figures (c) and (d) are the energy diagrams of a TFET at OFF and ON states.

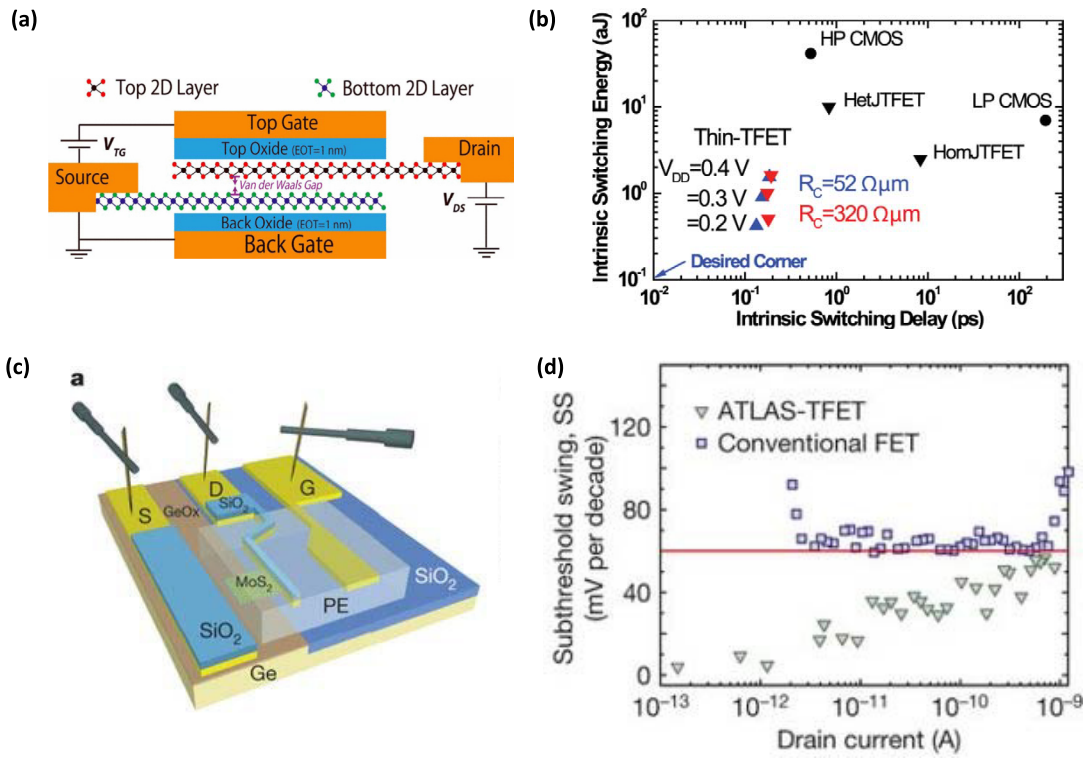

Figure 8. TFETs based on 2D TMDs. (a) Schematic device cross section of a thin-TFET [130]. (b) Intrinsic switching energy and delay for high performance (HP) CMOS, low power (LP) CMOS, heterojunction TFET (HetJTFET), homojunction TFET (HomJTFET), and thin-TFETs with $V_{DD} = 0.2, 0.3, 0.4$ V, and $R_C = 52, 320\ \Omega\mu$m [130]. (c) Schematic diagram showing the probing configuration for measurement of the characteristics of the ATLAS-TFET [133]. (d) SS as a function of drain current for an ATLAS-TFET (green triangles) as well as a conventional MOSFET (blue squares) at $V_{DS} = 0.5$ V. The red line demarcates the fundamental lower limit of SS of conventional FETs [133].

swing in this device is very high (~750 mV/decade) [125]. However, one should note that the presence of hysteresis can often mask the true SS of the device.

The key challenges in TFETs are the formation of atomically sharp transition between n-i-p regions and reduction of the interface traps. In recent years, 2D materials emerged that can be stacked on top of each other to form atomically sharp pn junctions. In addition, the 2D materials are free of surface dangling bonds, which potentially can reduce the interface states. Simulation of the TFETs based on 2D TMDs, their heterostructures and superlattices shows very

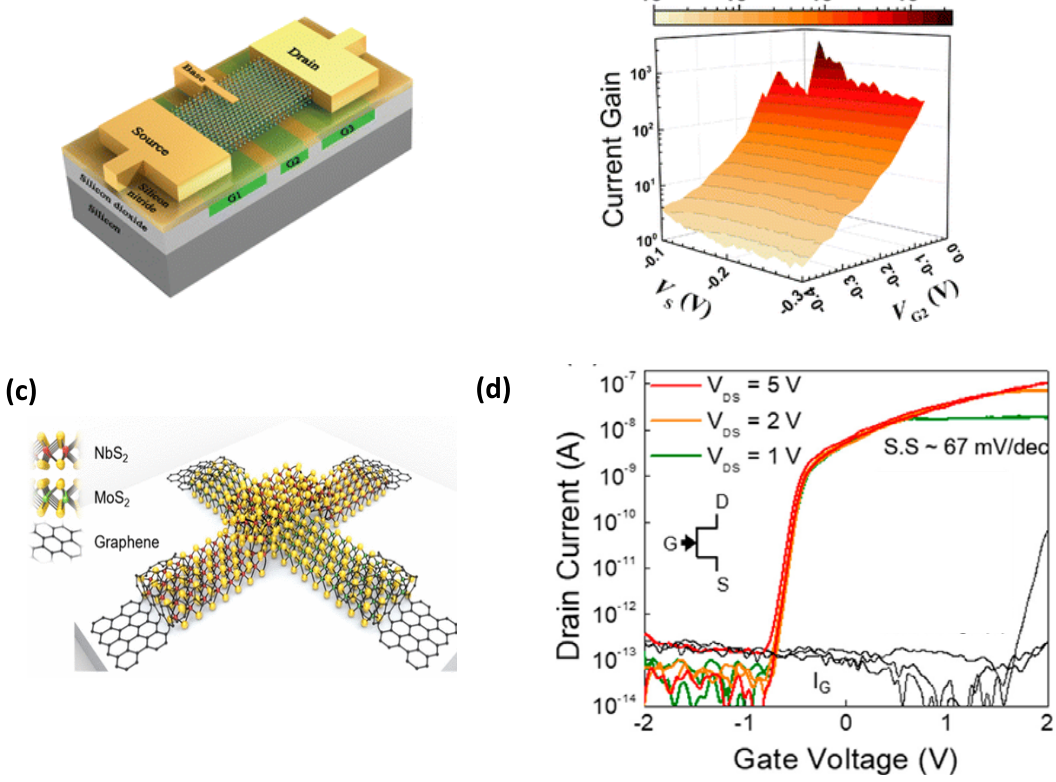

Figure 9. BJTs and MESFETs based on 2D TMDs. (a) Schematic and (b) map of BJT current gain β with varying V_S and V_{G2} determined at $V_D = 0.2$ V [134]. (c) A 3D schematic view of atomic layer NbS_2/MoS_2 MESFET [139]. (d) I_D–V_{GS} transfer and I_G–V_{GS} gate leakage curves of the MESFET, as measured with V_{DS} increase [139].

promising results [126]. For example, Ghosh's simulation of the lateral TFETs based on five MX_2 materials (MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2) shows steep SS (4 mV/decade) and high on-current (150 μA μm^{-1} at $V_d = 0.1$ V) [127]. Planar TFET based on narrow bandgap material Bi_2Se_3 (0.252 eV) can operate under ultralow supply voltage of 0.2 V, with an ON/OFF current ratio of 10^4 [128].

TFETs made of a vertical heterojunction of single-layer $MoTe_2$ and SnS_2 show on-currents >75 μA μm^{-1} and the inverse subthreshold slope reaches 25 mV/decade at 0 V [129], while TFETs based on $WSe_2/SnSe_2$ heterostructure can reach a steep subthreshold swing (SS) of ~14 mV/decade and a high on-current of ~300 μA μm^{-1} [130]. Li's simulation shows that 2D TFETs may outperform CMOS and III–V TFETs in terms of both switching speed and energy consumption at low supply voltages (figures 8(a) and (b)) [130]. Lu *et al* simulated TFETs based on MoS_2/WSe_2 superlattices and found that the on-current of the TFETs based on the superlattices is more than 4 orders of magnitude greater than that in TFETs based on MoS_2 or $MoSe_2$ homojunction [131]. However, there are very few experimental results of TFETs showing subthreshold swing below 60 mV/decade. The key challenge of the 2D TFETs is the interface states in the real devices, which can severely degrade subthreshold swing. TFETs based on $WSe_2/SnSe_2$ heterostructures with clean interfaces yield a subthreshold swing of 100 mV/decade for more than two decades of drain current at room temperature [132]. Recently, Sarkar *et al* demonstrated vertical TFETs based on highly doped germanium and atomically thin MoS_2 with solid polymer electrolyte as gate dielectric, which exhibit minimum subthreshold swing of 3.9 mV/decade and an average subthreshold swing of 31.1 mV/decade for four decades of drain current at room temperature, shown in figures 8(c)–(e) [133]. These TFETs will have broad applications from mobile devices to medical implantable devices and data centers. The availability of a large library of 2D materials would offer ideal materials alignment needed for TFET applications. Low *et al* recently surveyed a wide range of 2D semiconductor band alignments and identified combinations with momentum matched type III heterostructures [77]. Type III band alignment is most favorable in terms of yielding a larger ON state current.

2.2.4. Bipolar transistor

A traditional bipolar transistor (BJT) typically consists of a pnp or npn junction. Unlike MOSFET, where only one type (unipolar) of carrier dominates the current transport in a given device, in BJT, both types (bipolar) of carrier are involved. BJT is commonly used for current amplification. Traditionally the npn and pnp junctions were fabricated by local doping of the

silicon wafers. Recently, Agnihotri *et al* demonstrated a BJT device based on WSe_2 by using buried gates to electrostatically create doped regions with back-to-back pn junctions. These WSe_2 bipolar transistors show a current gain of 1000 and photocurrent gain of 40, shown in figures 9(a) and (b) [134]. The key advantage of this new type of the bipolar transistor is the re-configurability, where an npn BJT can be dynamically reconfigured into a pnp BJT using electrical signal, a feature non-existent in traditional semiconductor based BJT. In addition to these homojunction bipolar transistors, heterojunction bipolar transistors (HBT) based on TMDs were also explored. HBTs based on 2D TMDs can address several challenges in traditional HBTs based on bulk materials, such as dopant diffusion, lattice match restriction and dislocation propagation. Lin *et al* demonstrated lateral HBT based on p-WSe_2/n-MoS_2 junctions with current gain of around 3 [135]. Lee *et al* fabricated vertical HBTs based on n-MoS_2/p-WSe_2/n-MoS_2 stacks, which show very high current gain (~150) [136]. These prototype bipolar devices open a new application for 2D heterostructures in analog and high-frequency electronics.

2.2.5. Junction field-effect transistor (JFET)

JFET uses the depletion in a pn junction to control the current in the channel. The depletion-layer width of the pn junction can be varied by modulating a reverse-bias voltage applied to the junction. Traditional JFETs based on silicon were fabricated by forming the local doping. In 2D materials, these pn junctions can be formed by stacking n- and p-type TMDs or by combining TMDs with other materials, which have complementary doping types. Kim *et al* demonstrated an n-channel depletion-mode β-Ga_2O_3 junction JFET through van der Waals bonding with an exfoliated p-WSe_2 flake [137]. These heterojunction JFETs exhibited excellent transfer and output characteristics with a high ON/OFF ratio (~10^8) and low subthreshold swing (133 mV/decade). VdW JFETs based on n-MoS_2 and p-$MoTe_2$ were also demonstrated with ON/OFF current ratio up to 10^4 [138].

2.2.6. Metal semiconductor field-effect transistor (MESFET)

In a MESFET, a metal-semiconductor Schottky barrier instead of a pn junction is used for the gate electrode. As compared to JFETs, the potential advantages of MESFETs are low-temperature process, low gate resistance and good heat dissipation. Shin *et al* demonstrated vdW MESFETs based on metallic NbS_2 and semiconducting n-MoS_2, illustrated in figure 9(c). The Schottky-effect MESFET displays little gate hysteresis and an ideal subthreshold swing of 60––80 mV/decade due to low-density traps at the vdW interface, shown in figure 9(d) [139].

2.3. Memory devices

Semiconductor memory is a digital electronic data storage device. Random access memory (RAM) is semiconductor memory, which allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory. There are two types of RAM: volatile memory, which loses its stored data when the power to the memory chip is turned off, and nonvolatile memory, which preserves the data stored in it during periods when the power to the chip is turned off. Major types of volatile memory are dynamic RAM (DRAM) and static RAM (SRAM). The major types of nonvolatile memory are flash memory, resistive RAM (RRAM), ferroelectric RAM (FRAM), phase-change RAM (PCRAM), and magnetoresistive RAM (MRAM). Volatile memories can be faster than nonvolatile memories, while nonvolatile memories can consume less power and save the data while the power is off. Volatile memories are typically used as the main memory in the computers, while nonvolatile memories, such as flash memories, are typically used as solid-state hard drives, and in portable devices such as personal digital assistants (PDAs), USB flash drives, and removable memory cards used in digital cameras and cell phones.

2.3.1. SRAM

SRAM is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit. A typical SRAM cell is made up of six MOSFETs (2 pFETs and 4 nFETs). TMDs with sizable bandgap and atomically thin body, which provide excellent immunity to short-channel effects, are very attractive for future extremely-dense low-voltage SRAM arrays. Han *et al* demonstrated functional SRAM based on bilayer MoS_2 using direct-coupled FET logic technology, shown in figures 10(a) and (b) [140]. In order to form devices with different threshold voltages, the authors used metals with different work functions as the gate electrodes to form depletion-mode and enhancement-mode transistors. TCAD simulation reveals that monolayer TMDs with excellent device electrostatics and superior stability are promising for low-power SRAM applications, while the bilayer TMDs, with higher carrier mobility, are more suitable for high-performance SRAM applications [141].

2.3.2. DRAM

DRAM is a type of random access memory that stores each bit of data in a separate capacitor. The capacitor can either be charged or discharged. These two states are taken to represent the two values of a bit, conventionally called '0' and '1'. A typical DRAM cell consists of one transistor and one capacitor (1T1C). In this type of DRAM cell, the read is destructive and a write-back operation is needed. Recently Kshirsagar

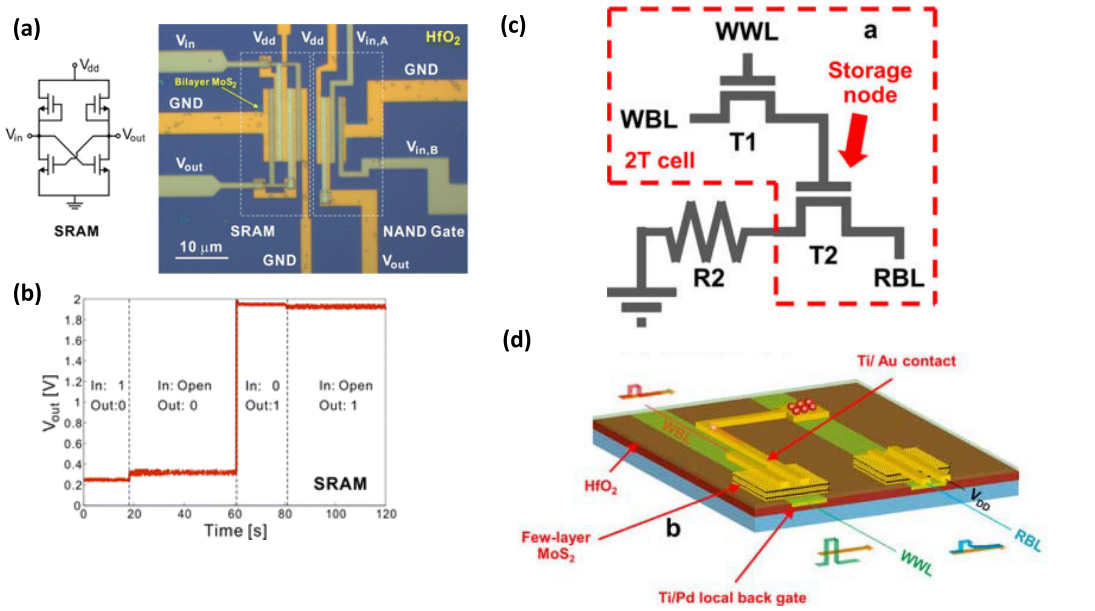

Figure 10. SRAM and DRAM based on 2D TMDs. (a) Optical micrograph, schematics of the electronic circuits, and (b) output voltage of a flip-flop memory cell (SRAM) based on MoS_2 [140]. (c) Circuit schematic and (d) illustration of 2T DRAM memory cell based on MoS_2 [142].

et al demonstrated a DRAM cell based on two MoS_2 transistors, shown in figures 10(c) and (d) [142]. In this DRAM cell, the read is non-destructive. In addition, since MoS_2 has wide bandgap (1.8 eV in monolayer) and high effective masses, which lead to extremely low OFF-state leakage currents, this new type of DRAM is promising for low-power applications [142].

2.3.3. Flash memory

Flash memory stores information in an array of memory cells made from floating-gate transistors. In the traditional flash memory, the floating gate is typically made of a polycrystalline silicon conductive layer. Bertolazzi *et al* demonstrated a floating gate memory device using graphene as the floating gate and MoS_2 as the channel, as shown in figures 11(a) and (b). Due to its 2D nature, monolayer MoS_2 is highly sensitive to the presence of charges in the charge trapping layer, which leads to a ratio of channel resistance (10^4) between memory program and erase states [143]. Cao *et al* had shown that employing multilayer graphene as floating gate can effectively reduce cell-to-cell interference (CTCI) and threshold voltage variation due to reduced floating gate thickness. In addition, due to the band offset between graphene and TMD layer, the stored electrons in the graphene floating gate are unlikely to leak out, which can help to prolong the retention of the memory cell [144]. The reverse device structure, where graphene serves as the channel and MoS_2 is used as the charge trapping layer, was also demonstrated [145]. Large memory window and stable retention were observed in these devices [145].

2.3.4. FRAM

FRAM utilizes ferroelectric polarization switching for data storage. In a FRAM cell, the dipoles tend to align themselves with the field direction when an external electric field is applied to the dielectric structure. The dipoles retain the polarization state after the electric field is removed. Therefore, FRAM is ideally nonvolatile. Typically, the memory cell in FRAM consists of 1 transistor (1T), or 1 transistor and 1 capacitor (1T1C). In the 1T1C structure, the read operation is destructive and a 'write-back' operation is needed, which can severely degrade the endurance of the memory cell. In the 1T structure, however, the read operation is nondestructive, which provides advantages including high endurance and low energy consumption. Lipatov *et al* fabricated ferroelectric memory based on MoS_2 on a lead zirconium titanate ($Pb(Zr,Ti)O_3$, PZT) substrate that was used as a gate dielectric, shown in figures 11(c) and (d). The MoS_2/PZT ferroelectric transistors exhibit a large hysteresis and high ON/OFF ratios. Interestingly, the authors found that this type of FRAM can be written and erased both electrically and optically [146]. Ferroelectric memory devices based on monolayer MoS_2 and aluminium (Al)-doped hafnium oxide (HfO_2) as the ferroelectric gate dielectric were also demonstrated [147]. These memory transistors show sizable memory window and clear wake-up effect [147]. Recently, Si *et al* demonstrated FRAM based on MoS_2 and 2D ferroelectric material $CuInP_2S_6$, which opens up a new route toward ferroelectric memories based on vdW heterostructures [148].

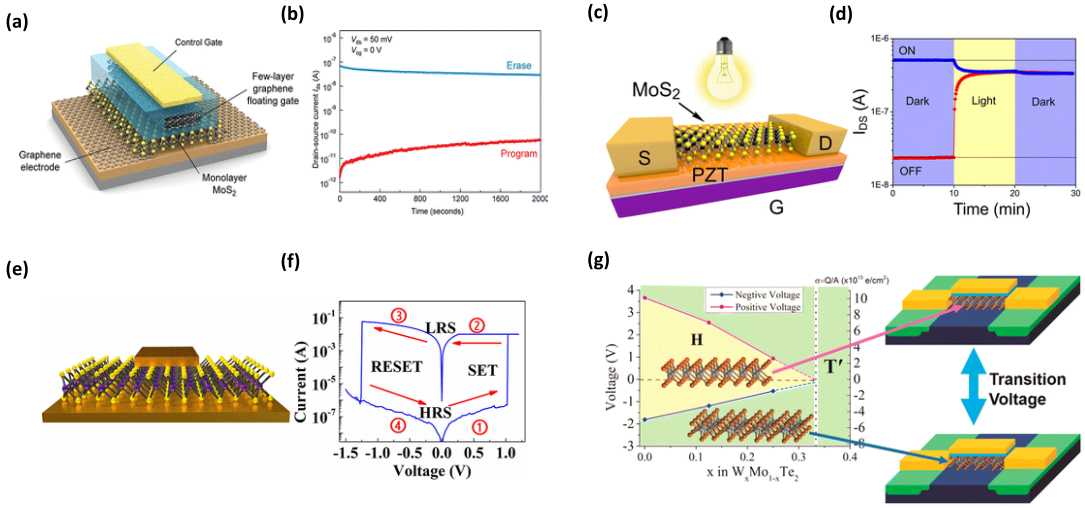

Figure 11. Nonvolatile memories based on 2D TMDs. (a) Three-dimensional schematic view of the memory device based on single-layer MoS_2 [143]. (b) Temporal evolution of drain-source currents (I_{ds}) in the erase (ON) and program (OFF) states. The drain-source bias voltage is 50 mV and the duration of the control-gate voltage pulse is 3 s [143]. (c) Schematic of and (d) effect of visible light illumination on the data retention characteristics of a MoS_2/PZT FeFET [146]. (e) Schematic and (f) typical *I*–*V* curves of monolayer TMD atomristors [150]. (g) Positive (pink) and negative (blue) voltage required to switch the relative stability of H-$MoTe_2$ and T′-$MoTe_2$ [157].

2.3.5. RRAM

RRAM is based on an array of memristors, where the high-resistance and low-resistance states are used to store data. Traditional memristors were mainly based on metal oxide, such as titanium oxide or tantalum oxide. Wang *et al* demonstrated a memristor based on a van der Waals heterostructure composed of graphene/$MoS_{2-x}O_x$/graphene. These memristors exhibit excellent switching performance with an endurance of up to 10^7 and a high operating temperature of up to 340 °C. The authors attribute the switching mechanism to the migration of oxygen ions in $MoS_{2-x}O_x$ [149]. Ge *et al* demonstrated vertical memristors based on various TMDs including MoS_2, WS_2, $MoSe_2$ and WSe_2, shown in figures 11(e) and (f). Stable nonvolatile resistance switching was observed in these single-layer atomic TMD sheets sandwiched between metal electrodes [150]. These memristors can be used as nonvolatile flexible memory fabrics and in brain-inspired (neuromorphic) computing.

2.3.6. PCRAM

PCRAMs are based on phase-change materials that exist in two or more phases with different properties [151, 152]. These phases typically correspond to different resistances which can be used to store data. There are mainly two types of PCM: metal oxides (such as VO_2 and NbO_2) which can undergo a Mott metal-to-insulator transition [153], and chalcogenide glasses (such as $Ge_2Sb_2Te_5$) which can have amorphous-to-crystalline phase transition [152]. It was discovered recently that Mo- and W-dichalcogenides can exist in several 2D phases (2H and 1T or 1T′ phase) [154, 155]. The energy differences between the H and T′ monolayer phases, for six pure MX_2 compounds (M = Mo or W, X = S, Se or Te), were calculated using DFT [25]. $MoTe_2$ and WTe_2 have the smallest energy difference between H and T′ phase, which makes them the best candidates for phase transitions in these 2D materials [25]. More interestingly, the energy difference between H and T′ is positive for $MoTe_2$, while it is negative for WTe_2, which means that $MoTe_2$ is stable in the 2H phase, while WTe_2 is stable in the 1T′ phase. Alloying these two materials can lower the energy barrier between these two phases and the transition temperature can be tuned continuously from 0 K to ~933 K [156]. In the past, the phase transition was mainly achieved by thermal effect (Joule heating and laser illumination). The high reset current and the heat dissipated to the surrounding materials consume a large amount of energy. It was discovered recently that 2D phase change materials such as $MoTe_2$ and $Mo_xW_{1-x}Te_2$ can achieve phase transition by electrostatic gating, shown in figure 11(g) [157–160]. Based on the theoretic calculation, the energy consumption per unit volume of the electrostatically driven phase transition in monolayer $MoTe_2$ at room temperature is 9% of the adiabatic lower limit of the thermally driven phase transition in $Ge_2Sb_2Te_5$ [161]. These results indicate that 2D TMDs are very promising for PCRAM applications.

3. Integrated circuits based on TMDs

Although TMD electronics are still in their early exploratory stage, significant progress has been made toward integrating these devices into circuits. Wang *et al* demonstrated an inverter, a NAND gate, an SRAM, and a five-stage ring oscillator using bilayer MoS_2 based on the direct-coupled transistor logic technology. These circuits comprise between 2 and 12 integrated transistors with bilayer MoS_2 channel. Both

enhancement-mode and depletion-mode transistors were fabricated by using gate metals with different work functions [140]. Tosun *et al* demonstrated a complementary logic inverter based on WSe_2 flake [162]. High work function metal Pt was used as the contact metal for p-FET to facilitate the hole injection, while potassium was used to form degenerately doped n^+ contacts for n-FET to enhance electron injection. These inverters show a dc voltage gain higher than 12 [162]. Yu *et al* demonstrated a high-performance WSe_2 CMOS inverter using F_4TCNQ for n-type doping. These inverters show large voltage gain (~38) and small static power (picowatts) [163]. Wachter *et al* moved one step further and demonstrated a 1-bit implementation of a microprocessor using a MoS_2 [164]. The microprocessor can execute user-defined programs stored in an external memory, perform logical operations and communicate with its periphery circuits [164]. Integrated circuits based on the combination of various 2D TMDs or combining 2D TMDs with other materials have also been demonstrated. Yu *et al* demonstrated a complementary inverter by vertically stacking graphene, $Bi_2Sr_2Co_2O_8$ (p-channel), graphene, MoS_2 (n-channel) and a metal thin film in sequence [165]. Cho *et al* reported on the design of a complementary inverter, based on a MoS_2 n-type transistor and a WSe_2 p-type transistor [166]. Pezeshki *et al* employed a direct imprinting technique to fabricate inverters using α-$MoTe_2$ for the p-channel FETs and MoS_2 for the n-channel FETs [167]. To avoid ambipolar behavior and produce α-$MoTe_2$ FETs with clean p-channel characteristics, the authors have employed the high work function metal platinum for the source and drain contacts [167]. These inverters show voltage gains as high as 33, switching delay of 25 μs, and static power consumption of a few nanowatts.

Beyond the planar integrated circuit, 3D integrated circuits were also explored recently. 3D integration can bring various types of circuits in close proximity in the vertical direction to achieve performance improvements with reduced power and a smaller footprint than the conventional 2D processes. A processor-in-memory (PIM) architecture has been proposed recently, wherein a logic layer is 3D stacked with a DRAM layer to reduce energy consumption related to data transfer while simultaneously increasing the performance [168, 169]. In the past, 3D integration was mainly achieved by stacking wafers/dies and interconnecting them vertically, using through-silicon vias (TSVs). This technique has the drawbacks of high cost, long vertical distance between the wafers, and the very limited number of wafers that can be stacked. 2D materials can be stacked layer-by-layer and address this issue [51]. Yang *et al* demonstrated the first 1-transistor-1-resistor (1T1R) memory cell using the atomically thin MoS_2 FET and RRAM [170]. Yang *et al* demonstrated a monolithic 3D image sensor, which consists of large-area monolayer MoS_2 phototransistor array on top of silicon logic/memory circuits. This 3D monolithic integration of 2D TMD devices with traditional silicon circuits opens up a new route toward high-density and energy-efficient electronic and optoelectronic systems.

4. Conclusion and outlook

This paper provides a comprehensive overview of electronic devices based on 2D TMDs, ranging from two-terminal devices such as Esaki didoes and RTDs, to transistors such as TFETs and RF devices, and to memories. The unique properties of 2D materials, including atomically thin body, dangling bond-free surface, and atomically sharp heterojunction interface bring new features to the traditional devices. For example, TMD heterostructures with broken-gap band alignment can enable Esaki diodes with prominent NDRs, TMD heterogeneous pn junctions enable vertical TFETs with super-steep subthreshold slope, and TMD atomically thin body provides TMD transistors with superior immunity to short-channel effects. TMDs with low energy barrier between 1H and 1T phase, such as $MoTe_2$ and $Mo_xW_{1-x}Te_2$ alloys, are very attractive for phase-change memories. The phase transition tunable by electrostatic gating can enable PCRAMs with ultralow energy consumption. In addition, 3D monolithic integration of the 2D electronic devices opens up a new route toward high-density and low-power applications. However, there are many limitations and challenges in 2D TMD electronics, such as large-scale high-quality synthesis of TMDs and contact resistance issues. Much research and development effort is still needed before these materials and devices are ready for mainstream applications. If these efforts are successful, 2D electron devices can potentially have broad applications from data centers to mobile devices, THz detectors, and wearable electronics.

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