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Three-Terminal Graphene Negative Differential Resistance Devices

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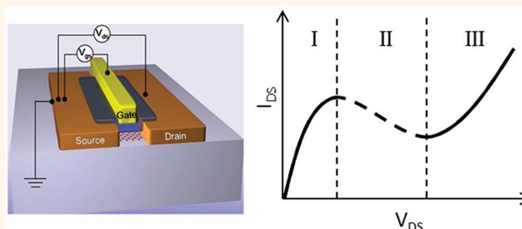
ABSTRACT



A new mechanism for negative differential resistance (NDR) is discovered in three-terminal graphene devices based on a field-effect transistor configuration. This NDR effect is a universal phenomenon for graphene and is demonstrated in devices fabricated with different types of graphene materials and gate dielectrics. Operation of conventional NDR devices is usually based on quantum tunneling or intervalley carrier transfer, whereas the NDR behavior observed here is unique to the ambipolar behavior of zero-bandgap graphene and is associated with the competition between electron and hole conduction as the drain bias increases. These three terminal graphene NDR devices offer more operation flexibility than conventional two-terminal devices based on tunnel diodes, Gunn diodes, or molecular devices, and open up new opportunities for graphene in microwave to terahertz applications.

KEYWORDS: negative differential resistance · graphene · field-effect transistor

Negative differential resistance (NDR) devices are electronic components with nonohmic current−voltage characteristics and are used in a wide array of applications including frequency multipliers, memory, fast switches, and most importantly, high-frequency oscillators up to the THz range. Conventional NDR devices such as Esaki diodes, Gunn diodes, or molecular devices are two-terminal devices, and their operation principles are based on either quantum tunneling or intervalley carrier transfer.[1−12] While graphene NDR devices have been proposed using nanoribbons or p−n junctions in bilayer graphene,[13,14] demonstration of such effects in graphene-based devices remains elusive due to the difficulties in meeting the stringent operating conditions experimentally.

Here, we report on graphene NDR devices based on a three-terminal field-effect transistor (FET) configuration. Different from NDR effects previously demonstrated or proposed, NDR observed in these devices results from the ambipolar transport behavior of graphene, without relying on effects of quantum tunneling. These results not only provide a new mechanism for NDR, but may also lead to new opportunities and applications based on this effect. For example, these three-terminal devices offer a key advantage over their two-terminal counterparts because the gate electrode can be used to control the current density, the onset of NDR behavior, and the output power of the ac oscillation. Moreover, the availability of large-area graphene coupled with demonstrated wafer-size device fabrication schemes makes graphene NDR devices a practical and promising technology for high-frequency electronics beyond conventional field-effect transistor operations.[15−22]

RESULTS AND DISCUSSION

Graphene NDR devices studied here are based on a top-gated or bottom-gated FET configuration, as depicted by the schematic in Figure 1a. In this configuration, the gate voltage (V_{GS}) is used to modulate the channel carrier density and determine the current−voltage characteristics between the source and drain electrodes. In addition, the gate voltage also controls the drain voltage range (V_{DS}) of the NDR regime, as explained later. The main experimental results presented here are based on epitaxial graphene grown on a SiC wafer[23] using silicon nitride (Si_3N_4) as the top-gate dielectric.[24] These devices exhibit ambipolar transport, as characterized by the "V"-shape transfer curve (Figure 1b). The gate bias at the current minimum in Figure 1b is defined as the neutrality point voltage ($V_{GS} = V_{NP}$), where the changes in the electron and hole currents become equal as V_{GS} is varied. NDR is characterized by a negative slope in the I_{DS}−V_{DS}

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Received for review December 28, 2011 and accepted February 10, 2012.

Published online February 10, 2012
10.1021/nn205106z

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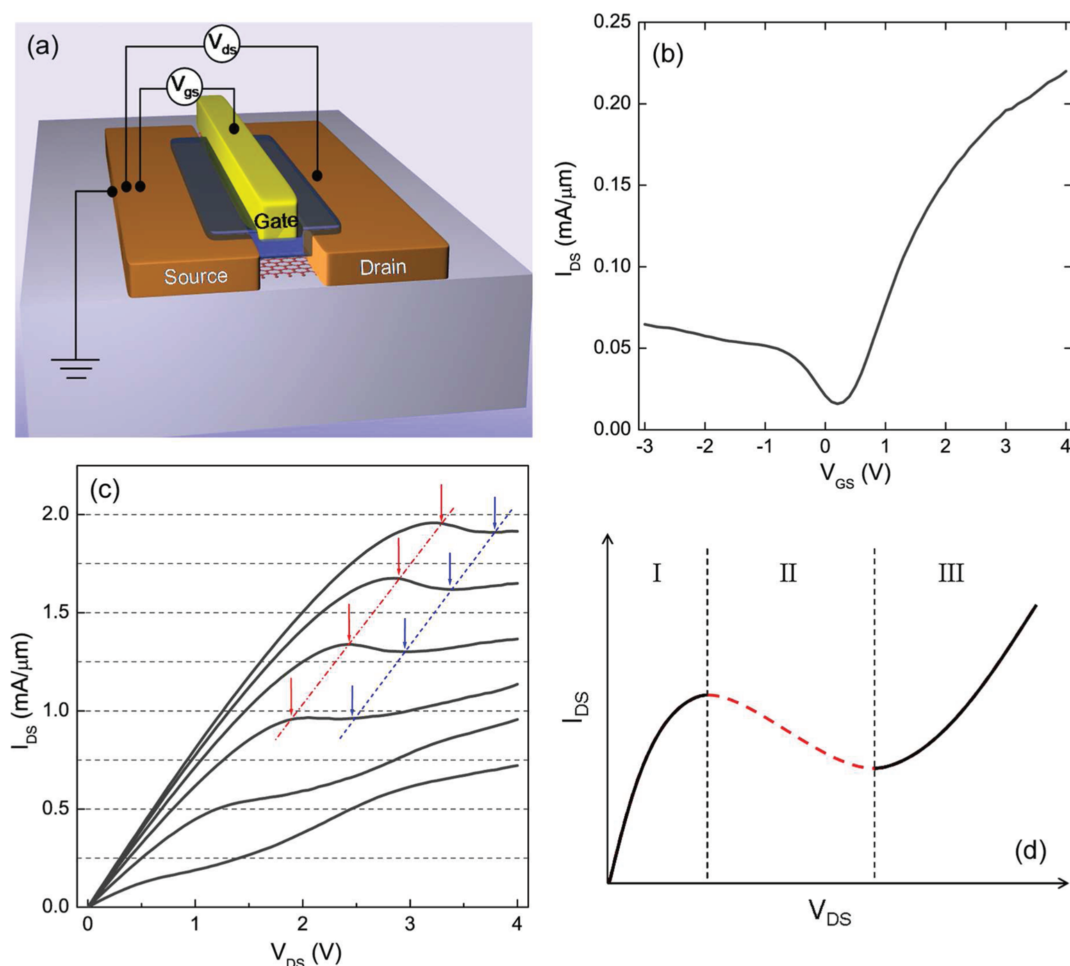

Figure 1. (a) Schematic of a three-terminal top-gated graphene NDR device. (b) Drain current (I_{DS}) measured as a function of gate voltage (V_{GS}) for a typical graphene transistor with a gate length of 3 μm. The drain bias is 0.1 V and the source is grounded. The current is normalized with respect to the total channel width. (c) I_{DS} as a function of V_{DS} of the 3 μm graphene device for top-gate voltages of 0−2.5 V in 0.5 V steps. Clear evolution of peaks (red arrows) and valleys (blue arrows) can be observed when V_{GS} changes. The maximum gate leakage current experienced during these measurements was 10 pA. (d) Schematic of the three transport regions in a graphene NDR device.

curve ($dI_{DS}/dV_{DS} < 0$), which can be clearly observed from the measured output characteristics of the graphene FET (Figure 1c), and this feature becomes more pronounced as the gate voltage increases. It is important to note that this NDR phenomenon is not specific to the type of graphene or the dielectric materials used. Instead, it is a unique but general feature in graphene devices under certain conditions. Similar NDR demonstrations are realized using CVD graphene with Si_3N_4 or HfO_2 gate dielectrics, as well as epitaxial graphene using an electrolyte gate dielectric (see Supporting Information).

The general features of an $I_{DS}-V_{DS}$ curve exhibiting NDR behavior is shown in Figure 1d. As the drain bias increases, the $I_{DS}-V_{DS}$ curves reach a local maximum and then decrease to a valley region before the current rises again. This NDR effect is associated with the ambipolar transport exhibited by graphene, where either electrons or holes can be the majority carrier depending on the bias configuration. NDR behavior can be qualitatively understood from the evolution of the carrier distribution in the graphene channel as the drain voltage varies, as depicted in Figure 2. Figure 2a shows a schematic band diagram of the graphene channel for a positive gate-to-source voltage (*i.e.*, $V_{GS} > 0$) and small drain-to-source bias ($V_{DS} \approx 0$). In this case, the dominant carriers in the channel are electrons injected from the source with a carrier density controlled by V_{GS}. Therefore, the channel resistance is nearly constant, and the device exhibits Ohmic-like $I_{DS}-V_{DS}$ behavior, corresponding to Region I in Figure 1d. As V_{DS} increases and becomes equal to V_{GS} (Figure 2b), the local Fermi energy at the drain coincides with the Dirac point. Since the local channel resistivity is inversely proportional to the local carrier density, most of the voltage drop occurs at the drain side because the channel resistance is highest at the drain. Figure 2c depicts the band diagram of the graphene channel when V_{DS} is $1.5V_{GS}$. It is noted that the dominant carriers close to the drain are holes injected from the drain, and the carrier density at the

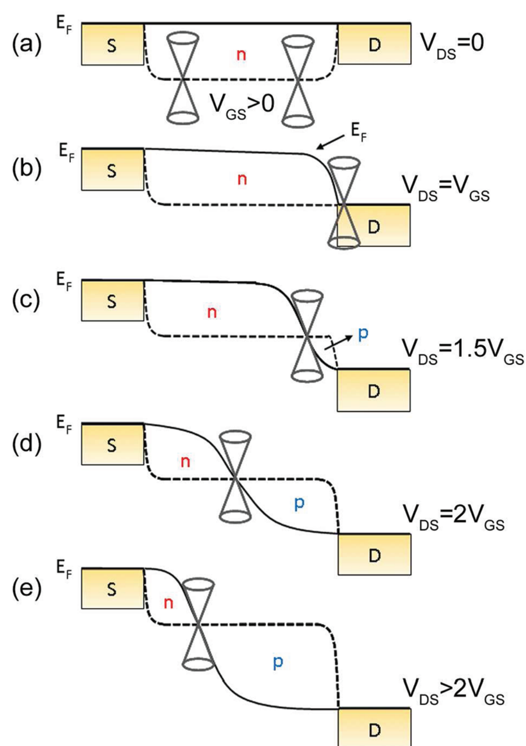

Figure 2. Band diagram schematics of the graphene channel at a constant gate voltage ($V_{GS} > 0$) and different drain biases: (a) $V_{DS} = 0$ V, (b) $V_{DS} = V_{GS}$, (c) $V_{DS} = 1.5V_{GS}$, (d) $V_{DS} = 2V_{GS}$, and (e) $V_{DS} > 2V_{GS}$. The dashed lines represent the position of the local Dirac point in the graphene band structure, and the solid lines represent the local Fermi energy along the channel. In schematic d, the band diagram also corresponds to the situation of $V_{GS} = V_{NP}$.

drain is determined by $V_{GD} = V_{GS} - V_{DS}$. As shown in Figure 2c, the transport in part of the graphene channel is dominated by hole carriers, and the Fermi energy passes through the Dirac point. At this pass-through point, the local resistivity is the highest along the channel, leading to most of the voltage drop close to this point. Compared to the band diagram in Figure 2b, it is evident that the total channel resistance in Figure 2c is higher because part of the electron-dominated channel is replaced by a hole-dominated region with a lower carrier density and higher resistance. This increase in the total channel resistance can result in a decrease in drain current with increasing drain bias, that is, the NDR behavior corresponding to the Region II in Figure 1d. The trend of increasing channel resistance continues until the distribution of electron and hole carriers becomes symmetric along the channel, or equivalently, when $V_{DS} = 2V_{GS}$ as shown in Figure 2d. Figure 2e depicts the band diagram when $V_{DS} > 2V_{GS}$. In this case, the total channel resistance is lower than that of Figure 2d due to two factors: (1) the decrease of hole-dominated channel resistance due to increasing hole carrier density and (2) replacement of part of the electron-dominated channel by the hole-dominated region with lower resistance. Therefore, when $V_{DS} > 2V_{GS}$, the drain current exhibits a superlinear behavior,

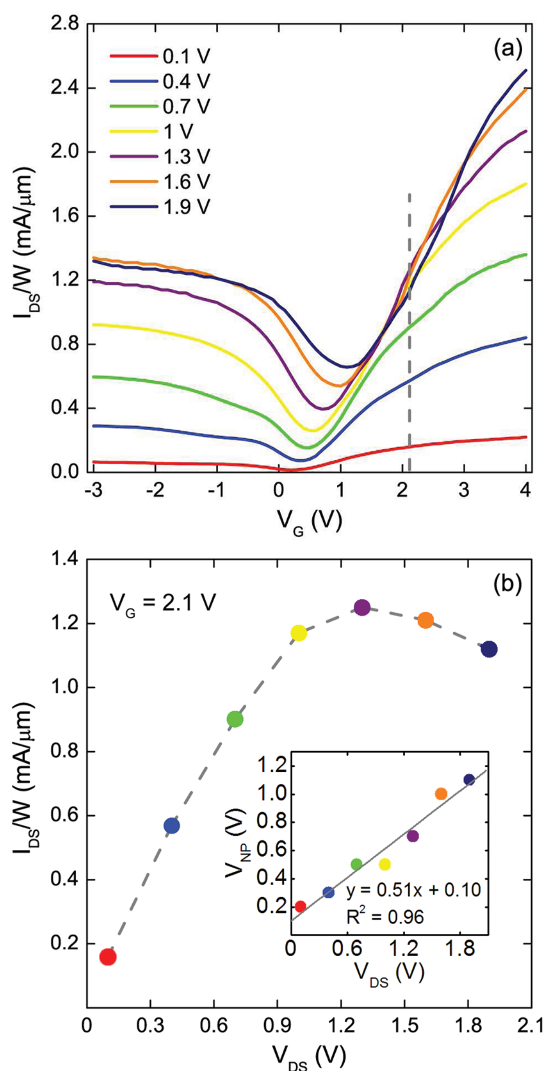

Figure 3. Device characteristics of an epitaxial graphene FET: (a) transfer characteristics for various drain biases; (b) measured current as a function of V_{DS} at $V_G = 2.1$ V, corresponding to the dashed line in panel a. Inset: Dependence of V_{NP} on V_{DS}. The solid line represents the linear fit with a slope of 0.51.

corresponding to the $I_{DS}-V_{DS}$ curves shown in Region III in Figure 1d.

NDR effects in graphene devices can also be qualitatively understood based on charge neutrality conditions at different drain biases. When V_{DS} increases (decreases), the transfer curve undergoes a shift in the positive (negative) bias direction, as marked by a distinct drain voltage dependence of V_{NP}. For instance, Figure 3a shows measured transfer characteristics of a graphene transistor for different drain biases, where V_{NP} increases with rising V_{DS}. This V_{NP} shift is a unique property of ambipolar transport and accounts for the change of carrier types and density distribution along the channel as V_{DS} varies.[25,26] More importantly, this shift of V_{NP} leads to convergence and crossing of the transfer curves in the electron branch, resulting in NDR phenomena within a range of gate voltages as highlighted by the dashed line

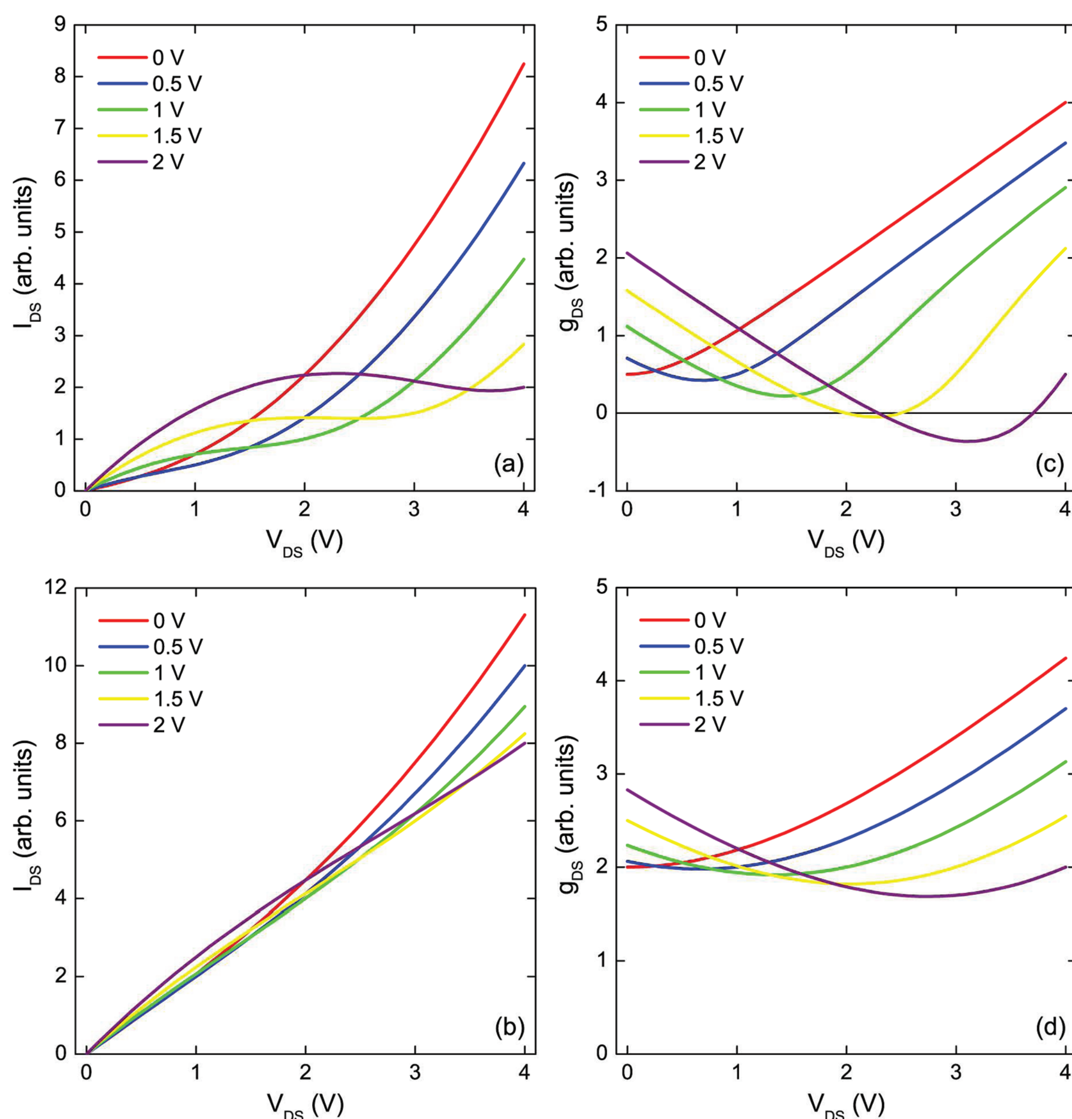

Figure 4. Modeled output characteristics and output conductances for graphene devices with different σ_{min}/K values at various gate voltages (V_{GS}). (a,c) $\sigma_{min}/K = 0.5$ V and (b,d) $\sigma_{min}/K = 2$ V. As outlined in the text, NDR is obtained when $\sigma_{min}/K = 0.5$ V, but not when $\sigma_{min}/K = 2$ V.

in Figure 3a that intersects the transfer curves at $V_{GS} = 2.1$ V. At this gate voltage, the device current decreases with increasing V_{DS} when $V_{DS} > 1.3$ V (see Figure 3b). For symmetric electron and hole branches, the amount of shift in V_{NP} is expected to be half of the drain bias. This is because at the neutrality point, the voltage difference between the gate and source should be equal to that of the gate and drain, as illustrated in Figure 2d. The inset of Figure 3b shows V_{NP} as a function of V_{DS}, where a linear dependence is clearly observed, and a slope of 0.51 is obtained from linear regression, in good agreement with this model. It is important to note that this shift differs from the threshold voltage shift observed in unipolar devices (*e.g.*, in a Si FET) with short channels, where the threshold voltage moves in the opposite direction of increased drain bias due to the short-channel effect.

To gain further insight into this behavior, a transport model for graphene NDR devices is developed, as summarized here and detailed in the Supporting Information. To a good approximation, the channel conductivity of a gated graphene device at small drain biases can be described by

$$\sigma(V_{GS}) = K\left[(V_{GS} - V_{NP})^2 + \left(\frac{\sigma_{min}}{K}\right)^2\right]^{1/2} \quad (1)$$

where $K = C_G \cdot \mu$ is the product of the gate capacitance (C_G) and carrier mobility (μ), and σ_{min} is the conductivity minimum. From symmetry arguments, as previously outlined and illustrated in Figure 2d, V_{NP} is dependent on V_{DS}, following the relation

$$V_{NP} = V_{NP}^0 + \frac{V_{DS}}{2} \quad (2)$$

where V_{NP}^0 is the gate voltage of the minimum current when V_{DS} approaches zero. On the basis of eq 2, the drain current at a finite V_{DS} can be expressed as

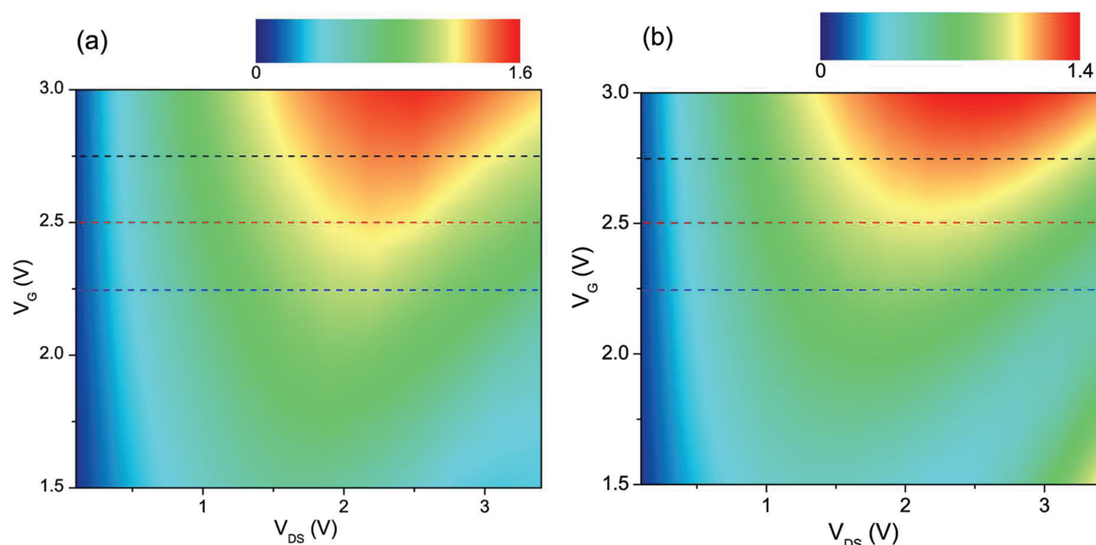

Figure 5. (a) Contour plot of a 3.5 μm gate graphene NDR device, where the device current is measured by sweeping the gate voltage at fixed drain bias steps. (b) Simulation of the device shown in panel a. Using measured values of carrier mobility, gate capacitance, minimum conductivity, and neutrality point voltage, along with reasonable values for the contact resistance and conduction asymmetry parameter, the measured results are described well by the model.

$$I_{DS} = \frac{W}{L}\cdot KV_{DS}\sqrt{\left(\tilde{V}_{GS} - \frac{1}{2}V_{DS}\right)^2 + \left(\frac{\sigma_{min}}{K}\right)^2} \quad (3)$$

where $\tilde{V}_{GS} = V_{GS} - V_{NP}^0$, and W and L are the channel width and length, respectively. The corresponding output conductance ($g_{DS} = dI_{DS}/dV_{DS}$) can therefore be expressed as

$$g_{DS} = \frac{K\cdot W}{L}\left(\frac{(V_{DS} - \tilde{V}_{GS})\left(\frac{1}{2}V_{DS} - \tilde{V}_{GS}\right) + \left(\frac{\sigma_{min}}{K}\right)^2}{\sqrt{\left(\tilde{V}_{GS} - \frac{1}{2}V_{DS}\right)^2 + \left(\frac{\sigma_{min}}{K}\right)^2}}\right) \quad (4)$$

This analytic expression for g_{DS} offers insight into the necessary conditions for the observation of NDR, which is characterized by a negative output conductance ($g_{DS} < 0$). eq 4 indicates that NDR occurs when

$$(V_{DS} - \tilde{V}_{GS})\left(\frac{1}{2}V_{DS} - \tilde{V}_{GS}\right) + \left(\frac{\sigma_{min}}{K}\right)^2 < 0 \quad (5)$$

or equivalently,

$$\frac{3}{2}\tilde{V}_{GS} - \sqrt{\frac{1}{4}\tilde{V}_{GS}^2 - 2\left(\frac{\sigma_{min}}{K}\right)^2} < V_{DS} < \frac{3}{2}\tilde{V}_{GS} + \sqrt{\frac{1}{4}\tilde{V}_{GS}^2 - 2\left(\frac{\sigma_{min}}{K}\right)^2} \quad (6)$$

It is evident that for a given ratio of σ_{min}/K, $\tilde{V}_{GS}$ needs to be larger than $(8)^{1/2}(\sigma_{min}/K)$ so that NDR can exist in a range of V_{DS} around $1.5\tilde{V}_{GS} = 1.5(V_{GS} - V_{NP}^0)$. This model provides a general description of the output characteristics of graphene transistors in terms of the ratio σ_{min}/K. For example, Figure 4 panels a and b show the modeled $I_{DS}-V_{DS}$ output characteristics for $\sigma_{min}/K = 0.5$ and 2 V, respectively. The corresponding output conductances as a function of V_{DS} calculated from eq 4 are plotted in Figure 4 panels c and d. As V_{DS} increases, g_{DS} decreases and exhibits a minimum at $V_{DS} \approx 1.5\tilde{V}_{GS}$. For $\sigma_{min}/K = 0.5$ V, the minimum g_{DS} becomes negative when $\tilde{V}_{GS} = 1.5$ V (Figure 4c), and the range of NDR becomes even more pronounced when $\tilde{V}_{GS}$ is increased to 2 V. In comparison, for $\sigma_{min}/K = 2$ V, the minimum g_{DS} is always positive up to $\tilde{V}_{GS} = 2$ V (Figure 4d), indicating an absence of the NDR effect within this operating voltage range.

While this analysis reveals the operating conditions necessary for the occurrence of NDR in an ideal graphene device, it is important to consider the impact of nonidealities in realistic devices such as contact resistance, conduction asymmetry between electrons and holes, and the bias dependence of the mobility and the minimum conductivity. In the presence of contact resistance (R_C), V_{DS} in eq 3 should be replaced by V'_{DS}, where $V'_{DS} = V_{DS} - I_{DS}R_C$ is the voltage drop across the graphene channel. It can then be shown that the total output conductance $g_{DS} = dI_{DS}/dV_{DS}$ is related to the channel output conductance $g'_{DS} = dI_{DS}/dV'_{DS}$ by

$$g_{DS} = \frac{g'_{DS}}{1 + g'_{DS}R_C} \quad (7)$$

Therefore, small values of R_C only slightly modify the magnitude of g_{DS}, and NDR behavior can be observed in the drain bias range determined by eq 6. Conduction asymmetry leads to different values of K for the electron and hole branches. In this case, the shift of V_{NP} will deviate from eq 2, and can be generalized as

$$V_{NP} = V_{NP}^0 + \alpha V_{DS} \quad (8)$$

where $0 < \alpha < 1$. Following similar derivations for eqs 4–6, it can be shown that NDR behavior exists

for a range of V_G and V_{DS} even when asymmetry is present. This is because the NDR effect occurs because V_{NP} moves in the same direction as V_{DS}, which remains valid even for asymmetric electron and hole transport. Increases in σ_{min} caused by impurities and decreases in K caused by high-energy scattering events at large drain biases will both have detrimental effects on NDR by increasing σ_{min}/K and consequently narrowing the NDR operation window.

By taking these factors into account, the modeled result is compared to the measured data. NDR conditions for a graphene FET are obtained from a contour plot of device current measured as a function of V_{DS} and V_{GS} (Figure 5a). Horizontal slices from this plot show the same behavior as in Figure 1c, where the drain voltage for the onset of NDR increases with V_{GS} as expected. Using the measured values of μ = 4500 cm^2/(V s), C_G = 350 nF/cm^2, σ_{min} = 0.55 mS/μm, and V^0_{NP} = -0.2 V for this device (σ_{min}/K = 0.35 V), in conjunction with α = 0.7 and R_C = 300 $\Omega\cdot\mu$m, the modeled results (Figure 5b) exhibit good agreement with the measurements.

CONCLUSIONS

While the transport behavior observed here is, in principle, applicable to all graphene materials, several conditions are needed for such NDR effects to be observed in realistic devices. As indicated above, NDR is mainly dependent on the ratio $\sigma_{min}/(C_G\cdot\mu)$, with the onset drain bias around $1.5(V_{GS} - V^0_{NP})$. Therefore, a heavily doped channel with V^0_{NP} far from zero can lead to V_{DS} values that are unrealistic. Typically, NDR is more readily observed in devices where the contact resistance is small compared to the channel resistance, and the gate has good electrostatic control over the channel. Though the shift of V_{NP} in graphene FETs is the main cause of NDR, other factors such as high-field induced scattering can lead to a smaller current increase as V_{DS} increases, and may therefore also facilitate the onset of NDR operation.[27] To demonstrate the universality of such NDR effects, graphene devices using various combinations of graphene materials and top-gate dielectrics have been fabricated and studied at a wide range of temperature (5 and 300 K), all showing clear and reproducible NDR behavior (Supporting Information). It should also be noted that this effect may not be exclusive to the type of transport exhibited by the device, as we have experimentally demonstrated NDR in the diffusive regime, and others have theoretically and computationally predicted NDR assuming ballistic transport.[28,29]

In summary, we have experimentally demonstrated prototypes of novel three-terminal graphene NDR devices and provided an analytic model to elucidate such NDR behavior. These results suggest a new operating mechanism for NDR, and open up new opportunities for graphene-based devices in future high-frequency applications beyond the conventional NDR device paradigm based on two-terminal diodes.

METHODS

Top-gated graphene transistors are fabricated on epitaxial graphene grown on SiC using conventional fabrication processes.[17] The detailed growth methods have been described elsewhere.[23] Graphene transistors are also fabricated on graphene grown by CVD on copper using both top-gated and embedded-gate structures (see Supporting Information for detailed device geometries). Different gate dielectrics such as Si_3N_4 deposited by plasma-enhanced CVD, HfO_2 deposited by atomic-layer deposition, and electrolyte dielectrics are also employed. The devices are defined using electron-beam lithography, where the active graphene area is patterned with oxygen plasma. The source and drain metal contacts are deposited by electron-beam evaporation at <10^{-7} Torr, and consist of a 20 nm Pd/40 nm Au metal stack. DC electrical characterization is carried out in a probe station (Lakeshore Inc.) both under vacuum (<10^{-6} Torr) and in air using an Agilent parameter analyzer B1500.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. The authors thank B. Ek, J. Bucchignano, D. Neumayer, X. S. Li, and H. Yan for technical assistance and K. Jenkins, T. Low, V. Perebeinos, C. Y. Sung, and A. Grill for discussion. The authors would also like to thank DARPA for partial financial support through the CERA program (Contract FA8650-08-C-7838). The views, opinions, and/or findings contained in this article are those of the author and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense. Approved for Public Release, Distribution Unlimited.

Supporting Information Available: Detailed transport model, experimental methods, and additional figures as described in the text. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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