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Novel vertical hetero- and homo-junction tunnel field-effect transistors based on multi-layer 2D crystals

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Abstract

Vertical hetero- and homo-junction tunnel FET (TFET) based on multi-layer black phosphorus (BP) and transition metal dichalcogenides are proposed and studied by numerical simulations employing the semi-classical density gradient quantum correction model. It is found that the vertical TFET based on BP can achieve high on-current (>200 μA μm^{-1}) and steep subthreshold swing (average value = 24.6 mV/dec) simultaneously, due to its high mobility, direct narrow bandgap, and low dielectric constant. We also found that the on-current in vertical TFETs based on $MoS_2/MoSe_2$ hetero-junction is two orders of magnitudes higher than the one in MoS_2 homo-junction TFET, due to the reduced effective bandgap in heterostructure with staggered band alignment. In addition, we present various design considerations and recommendations as well as provide a qualitative comparison with published data.

Introduction

In light of the excessive power dissipation issues plaguing the performance and scalability of IC devices, there has been a lot of interest searching for energy-efficient post-CMOS switches. Tunneling FET (TFET) [1–3]) is among the prime candidates for low power post-CMOS computing. The idea behind TFET (and other steep subthreshold slope (SS) devices) is to create an ideal abrupt switch—SS ~$[V_T - V_{G,OFF}]/\log[I_{ON}/I_{OFF}]$) much less than thermal limit (60 mV/dec)—therefore enabling the reduction of the operating voltage and overall power dissipation. Researchers have explored various TFET device architectures and design using group IV (e.g., [4, 5]), III–V semiconductor (e.g., [6, 7]), graphene/carbon based materials (e.g., [8]), and, most recently, 2D bilayer hetero-junction vertical TFET/tunnel diode based on vertical stack of monolayer transition metal dichalcogenides (TMDC) [9–13]. The use of 2D materials are particularly appealing for TFET design due to their sharp density of states, narrow thickness (which leads to excellent electro-static control), and absence of dangling bonds at the surface.

In this work, we propose the use of stacked multi-layered 2D black phosphorus (BP) and TMDC (e.g., MoS_2 and $MoSe_2$) homo-junction and type II (staggered) hetero-junction vertical TFET. The multi-layered hetero- (or homo-) structures can in principle be realized by stacking multiple monolayers of 2D materials on top of each other leading to a sequence of Van der Waal (vdW) bonded layered junctions/super-lattice with no interface states. One key advantage of stacking multilayered 2D crystal is that it facilitates tuning of electronic bandgap. A recent report suggested that careful selection of multilayer stacking may lead to the formation of direct bandgap, hence altering the electronic and optical properties [14], creating an additional knob to tuning TFET performance, particularly when combined with strain engineering. BP is particularly attractive as it has electronic properties in between graphene and TMDC—direct bandgap in both bulk (0.3 eV [15]) and monolayer (2 eV), high mobility, and low dielectric constant [15]. As compared to monolayer TMDC (which generally have direct bandgap), multi-layer TMDC have higher valley degeneracy and smaller indirect bandgap. Using the Sentaurus TCAD, we examine the performance of BP and TMDC multilayer hetero-/homo-junction TFET and explore various device engineering schemes to enhance performance. Additionally, we provide a

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qualitative comparison of our simulated devices with published TFET results.

Methods

We use the Synopsys Sentaurus TCAD [16] tool to perform self-consistent simulations of 2D vertical TFET. The band-to-band tunneling (BTBT) underlying the TFET operation is modeled using the dynamic non-local path band-to-band model, implemented in Sentaurus. This model takes into account the nonlocal generation of electrons and holes caused by direct and phonon-assisted BTBT processes. Since relevant tunneling parameters of the simulated 2D multilayer materials are not readily provided in Sentaurus, we use published results obtained from either experimental data [7, 15, 17, 18] or *ab initio* theoretical calculations [19–25] as summarized in table 1. The bandgap values used were extracted from published GW calculations, a well-established hybrid method that incorporates density functional theory (DFT) with Green's function and is well known for correcting the bandgap problem in standard DFT simulation. We particularly adopt the GW bandgap from Jiang *et al* [19] for TMDC and Tran *et al* [22] for BP, as they have both demonstrated that their estimated bandgaps are consistent with relevant experimental data. For the BP case [22] computed the bandgap variation as a function of layer thickness. Using their data, we have estimated values for the bandgap that correspond to our simulated thickness. In the absence of experimentally verifiable theoretical data for the exact multilayer TMDC thickness considered here , we adopt bulk-like bandgap values from [19] to model our multilayer TMDC since we expect that the bandgap for the thickness considered in this work would be closer to bulk property than monolayer. Additionally, it is worth noting that for the case of the multilayer TMDCs (with indirect minimal bandgap), we have also included the influence of the second and third minimal bandgaps corresponding to the nearby satellite indirect valley (~0.015 eV above the minimum bandgap for both MoS_2 and $MoSe_2$) and direct valley (~0.87 eV and ~0.73 eV above the minimum bandgap for MoS_2 and $MoSe_2$, respectively) on transport. We have used the same effective masses for both the MoS_2 and $MoSe_2$ (table 1) since the published theoretical results show little discrepancy (<10%) between them [26]. In order to take into account the highly anisotropic nature of BP, we use published in-plane effective masses, m_x and m_y, from previous experimental work [7, 18] and compute the average effective mass m_{xy} by applying the reciprocal law —$m_{xy} = \left(\frac{1}{m_x} + \frac{1}{m_y}\right)^{-1}$, assuming the charges flow equally in x and y directions.

The simulated device structures consists of 75 nm long metal gate (25 nm underlap +50 nm channel overlap) with asymmetric top and bottom work-function fabricated on top a 3 nm HfO_2 gate dielectric ($\epsilon_{ox} = 25$). The lateral offset between the n- and p-region is adopted to diminish source/drain leakage current. The source (P+) and drain (N+) contact is doped with $1 \times 10^{20}\ cm^{-3}$ boron and arsenic atoms, respectively. The channel is doped with either: $N_{ch} = 1 \times 10^{14}\ cm^{-3}$ (for the homogeneously doped TFET) or $N_D = N_A = 1 \times 10^{18}\ cm^{-3}$ (for both the n-type and p-type homo/hetero-junction TFET). The total channel thickness is set to 5 nm—each n-/p-layer is 2.5 nm thick, which corresponds to about five atomic layers. Table 1 provides a summary of the relevant materials parameters. The simulated devices are calibrated with a 1-D Schrödinger solver to mimic the influence of quantum confinement effect on the device electrostatic using the density gradient model.

Results and discussion

Figure 1 compares the performance of three TFET devices: homogeneous, np homo-junction, and hetero-junction TFET. The np homo-junction TFET provides higher I_{ON} as compared to the uniformly doped homogeneous TFET. This is mainly attributed to the narrower tunneling barrier and sharper transition between n and p region of the np homo-junction device. Additionally, the built-in potential of the np homo-junction leads to lower threshold voltage as compared to the homogeneous TFET. In order to further boost the on-current density, we employ multi-layer type II heterojunction TMDC TFET with MoS_2 as the n-channel and $MoSe_2$ as the p-channel. The band offsets between MoS_2 and $MoSe_2$, bandgap, and dielectric constant of $MoSe_2$ are all obtained from published theoretical results on multilayer TMDC (table 1). As summarized in figure 1, our simulated results indicate that, the on-current of the MoS_2/$MoSe_2$ hetero-junction TFET (with identical off-current and thickness) is two orders of magnitudes higher than that of the homogenously doped np homo-junction MoS_2 TFETs. The staggered hetero-junction provides lower effective barrier height across the n–p junction to facilitate the tunneling process while at the same time maintaining higher bandgap at the channel and source/drain region to mitigate the generation–recombination leakage current. The use of lateral offset (i.e., underlap) between the n- and p-layer (figure 1(b)) is essential for TFET design as it suppresses the lateral tunneling window along the channel and hence suppressing parasitic leakage current (figure 2). In order to quantify the reduction of current due to underlap region, we plot the drain current for both BP and MoS_2 with and without the underlap region (figures 2(a) and (b)). We observe that the lateral tunneling, due to the absence of the underlap region, is more pronounce for the BP case largely due to the lower bandgap of BP (compared to MoS_2),

Table 1. Parameters for tunneling calculation.

	m_{eff} (e) [7, 18, 19]	m_{eff} (h) [7, 18, 19]	E_g (eV) [7, 21, 22]	Dielectric constant (ϵ_0) [15, 17, 24]	Electron affinity [17, 19, 22]	D_{ac} (eV/m) [23]	ε_{op} (meV) [20, 25]
MoS_2	$m_z = 100$ (K), 0.49 (Λ)	$m_z = 1.73$ (K), 0.8 (Γ)	1.2 (indirect (Λ)), 1.215 (indirect (K)), 2.07 (direct)	4.8	4.2	4.4×10^{10} (indirect (Λ))	14.5 (indirect (Λ)) 23.1 (indirect (K))
$MoSe_2$	$m_{xy} = 0.46$ (K), 0.62 (Λ)	$m_{xy} = 0.45$ (K), 0.62 (Γ)	1.1 (indirect (Λ)), 1.115 (indirect (K)), 1.83 (direct)	6.9	3.92	4.8×10^{10} (in direct (K))	8 (indirect (Λ)) 14 (indirect (K))
Black phosphorus	$m_z = 0.2$, $m_{xy} = 0.07$	$m_z = 0.4$, $m_{xy} = 0.1$	0.8 (direct)	8	4.2	No phonons involved	

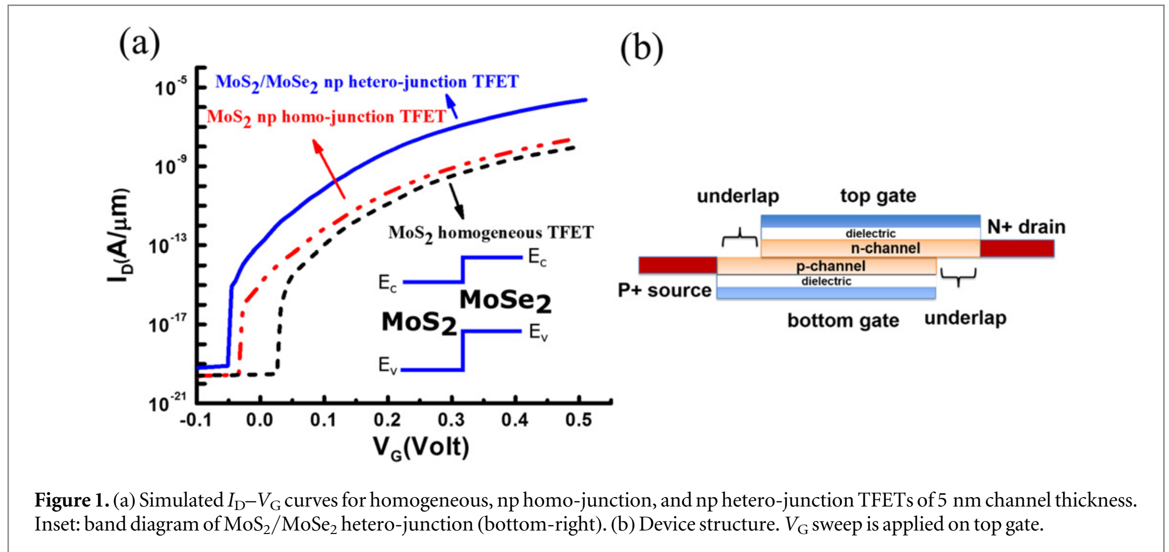

Figure 1. (a) Simulated I_D–V_G curves for homogeneous, np homo-junction, and np hetero-junction TFETs of 5 nm channel thickness. Inset: band diagram of $MoS_2/MoSe_2$ hetero-junction (bottom-right). (b) Device structure. V_G sweep is applied on top gate.

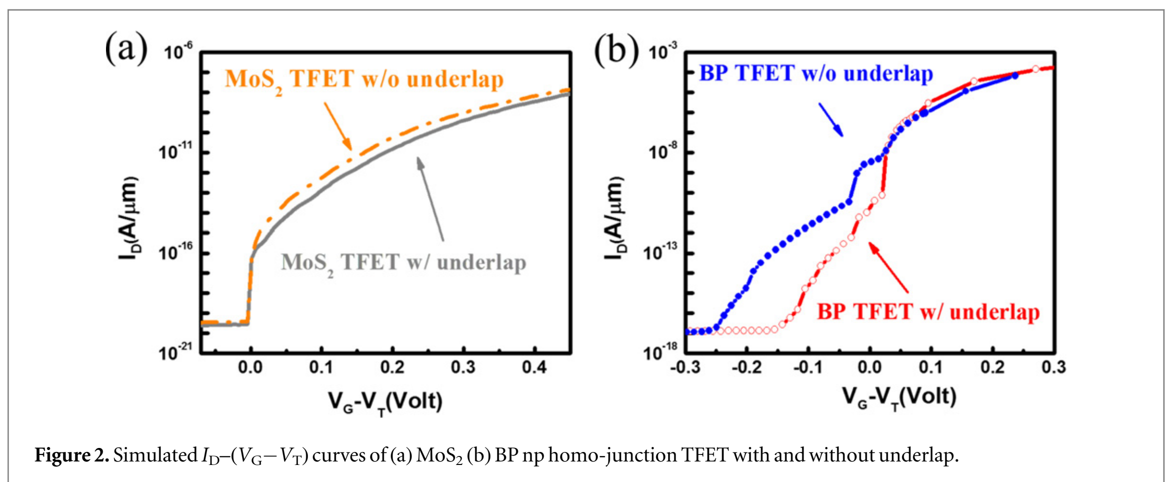

Figure 2. Simulated I_D–(V_G-V_T) curves of (a) MoS_2 (b) BP np homo-junction TFET with and without underlap.

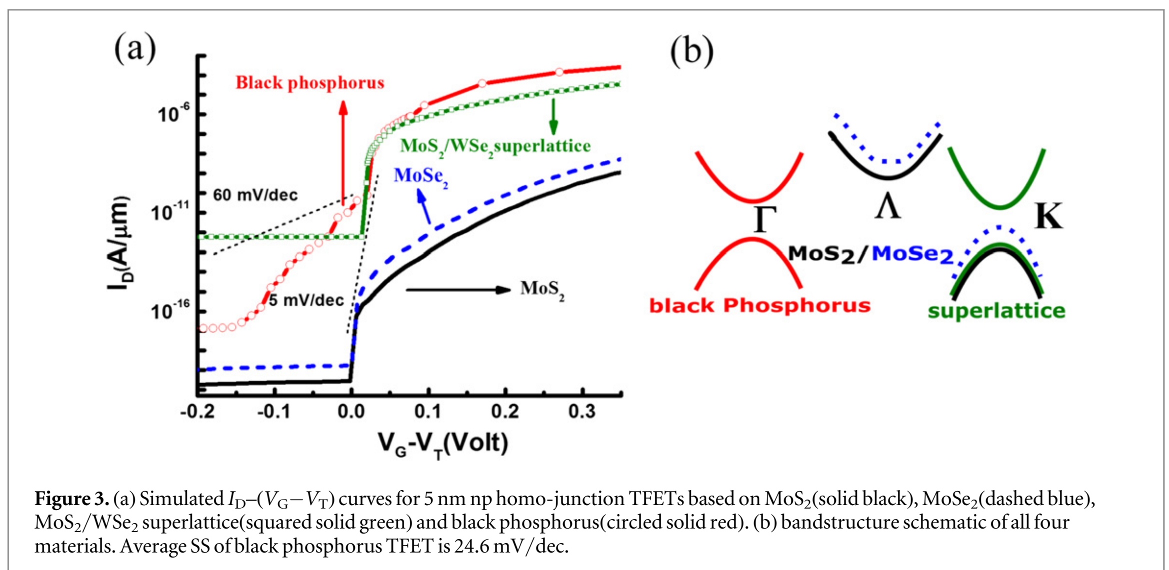

Figure 3. (a) Simulated I_D–(V_G-V_T) curves for 5 nm np homo-junction TFETs based on MoS_2(solid black), $MoSe_2$(dashed blue), MoS_2/WSe_2 superlattice(squared solid green) and black phosphorus(circled solid red). (b) bandstructure schematic of all four materials. Average SS of black phosphorus TFET is 24.6 mV/dec.

hence facilitating the tunneling process. Figure 3 shows that the on-current of the BP (direct bandgap) device is 4–5 orders of magnitude higher than the indirect bandgap MoS_2 and $MoSe_2$ devices. This is expected since the BTBT current is generally lower for indirect bandgap materials due to the tunneling transition requiring additional particle (phonon) to compensate the momentum offset between the

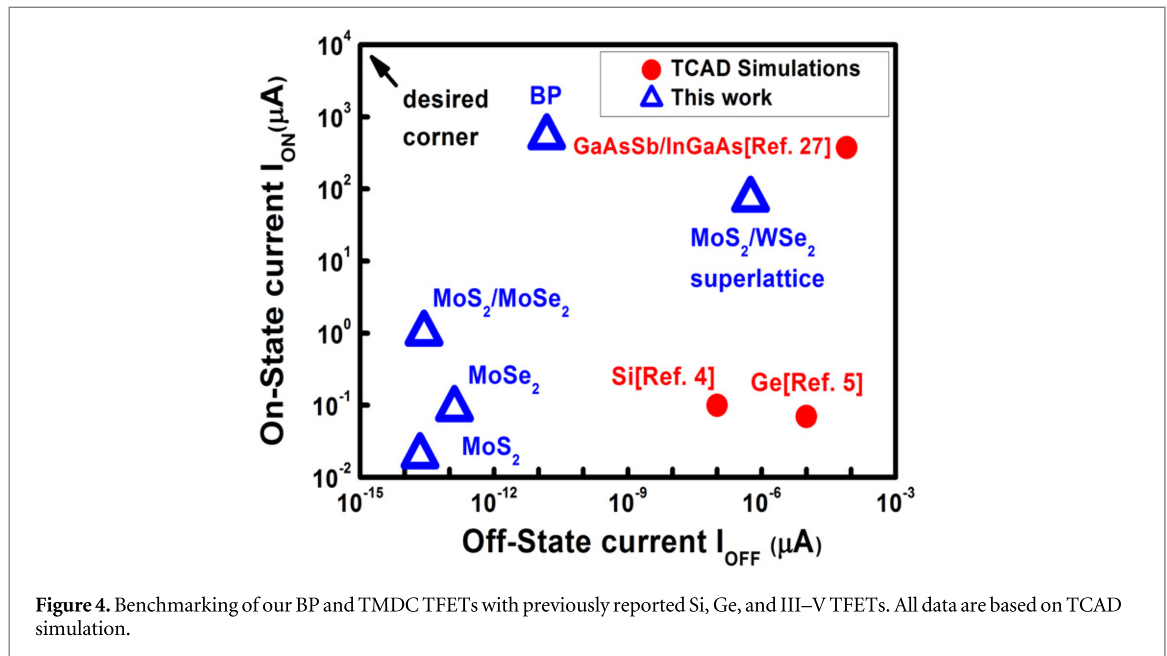

Figure 4. Benchmarking of our BP and TMDC TFETs with previously reported Si, Ge, and III–V TFETs. All data are based on TCAD simulation.

conduction and valence bands. Recently published first principle simulation has demonstrated the feasibility of designing direct bandgap multilayer TMDC–TMDC heterostructure by carefully choosing the ratio of the mono-layers [14]. We probe this as a thought experiment, by modeling the MoS_2 and WSe_2 as a direct bandgap ($E_g = 0.68$ eV) multilayer heterostructure. As shown in figure 3, we see a substantial increase in current (>4 orders of magnitude) albeit being lower than that of BP due to the differences in effective mass and bandgap. Figure 4 summarizes the results presented in this work and compares it with reported data (using the Sentaurus TCAD simulations) for Si [4], Ge homogeneous TFET [5] and III–V heterojunction TFET [27]. Note that the prospect of using multilayer TMDC to form direct gap vdW superlattice is very promising and shows a substantial improvement in on-current and a reasonable degradation in off-current. We can in principle optimize the off-current by using the layer thickness to tune the bandgap, and/or resort to staggered hetero-junction structure.

Conclusions

We have presented a computational study of multi-layered homo-/hetero-junction MoS_2, $MoSe_2$, and BP TFET devices using the Sentaurus TCAD software. Our finding indicates that multilayered BP is particularly promising ($I_{ON} > 200\ \mu A\ \mu m^{-1}$; avg. SS = 24.6 mV/dec) as compared to the TMDC based TFETs, due to its direct narrower bandgap and higher mobility. The contingency of constructing multi-layered 2D direct gap vdW superlattice TMDC is very promising and will provide ways to substantially enhance TFET performance. Benchmarking our work with recently published data show that 2D multi-layered direct gap vertical TFET design is a strong candidate for low-power application.

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