

# Nonconventional Analog Comparators Based on Graphene and Ferroelectric Hafnium Zirconium Oxide

Jialun Liu<sup>®</sup>, Hojoon Ryu<sup>®</sup>, and Wenjuan Zhu<sup>®</sup>, *Senior Member, IEEE* 

Abstract—Unlike transitional semiconductors, graphene has zero bandgap and symmetric electron/hole transport, which leads to unique V-shaped transfer characteristics. Using this property, we design and demonstrate a new type of comparator, which can calculate the absolute distance between two signals, |A - B|, directly. Dual-gate graphene transistors with ferroelectric hafnium zirconium oxide are fabricated to serve as the basic units of the comparators. We show that the remanent polarization of the ferroelectric hafnium oxide can reach  $\sim$  30  $\mu$  C/cm<sup>2</sup> and the output current of the comparator can serve as a scalar indicator of the similarity level between two signals. The embedded ferroelectric layer can store the reference signal in situ, which will reduce the energy consumption and latency related to the data transport. Furthermore, we demonstrate the feasibility of using ferroelectric graphene comparator in image classification and motion detection. Using the k-nearest neighbors (KNNs) algorithm, we show that the graphene comparator arrays can recognize the handwritten digits in the modified national institute of standards and technology (MNIST) data set with over 80% accuracy. These ferroelectric graphene comparators will have broad applications in robotics, security system, self-driving vehicles, and sensor networks.

*Index Terms*— Ferroelectric hafnium oxide, graphene, image classifier, in-memory analog computing, motion detection.

### I. INTRODUCTION

SILICON transistor is typically unipolar (either n-type or p-type), where the drain current changes monotonically with gate voltage [1], [2]. As illustrated in Fig. 1(a), the drain current difference between the two operating points (A and B) is proportional to the gate voltage difference:  $I_B - I_A \propto V_B - V_A$ , where  $V_A$  and  $V_B$  are the gate voltages, and  $I_A$ 

Manuscript received December 5, 2020; accepted January 3, 2021. Date of publication January 22, 2021; date of current version February 24, 2021. This work was supported in part by the National Science Foundation (NSF) under Grant ECCS 16-53241 CAR and in part by the Office of Naval Research (ONR) under Grant NAVY N00014-17-1-2973. The work of Hojoon Ryu was supported by the Kwanjeong Educational Foundation. The review of this article was arranged by Editor B. K. Kaushik. (Jialun Liu and Hojoon Ryu contributed equally to this work.) (Corresponding author: Wenjuan Zhu.)

Jialun Liu is with the Department of Electrical Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

Hojoon Ryu is with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

Wenjuan Zhu is with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA (e-mail: wjzhu@illinois.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3049757.

Digital Object Identifier 10.1109/TED.2021.3049757



Fig. 1. Illustration of the transfer characteristics of (a) silicon transistor, (b) ambipolar Schottky barrier transistor, and (c) graphene transistor.

and  $I_B$  are the drain current at operating points A and B, respectively. This type of transistor can easily implement the subtraction function (A - B), but is not convenient for calculating the absolute distance between two signals |A - B|. Some Schottky barrier transistors based on narrow bandgap semiconductors (such as black phosphorus and MoTe<sub>2</sub>) are ambipolar [3]–[7], where the transfer curves are U-shaped, as illustrated in Fig. 1(b). The drain current difference between the operating point B and charge neutrality point A is related to the absolute difference between the gate voltages  $|V_B - V_A|$ , if the gate voltage  $V_B > V_{\text{th}-n}$  or  $V_B < V_{\text{th}-p}$ , where  $V_{\text{th}-n}$ and  $V_{\text{th}-p}$  are the threshold voltages for the electrons and holes, respectively. If the gate voltage  $V_B$  is in between the two threshold voltages  $(V_{th-p} < V_B < V_{th-n})$ , the drain current difference between these two points is nearly zero:  $I_B - I_A \approx 0$ , which means that the transistor cannot perform |A - B| calculation in this voltage range. Graphene transistors have a V-shaped transfer characteristic due to the zero bandgap and symmetric electron/hole transport in graphene, as shown in Fig. 1(c). The drain current difference between operating point B and Dirac point A is  $I_B - I_A \propto |V_B - V_A|$  for nearly all gate voltages, which is ideal for the |A-B| calculation. This absolute distance function will be very useful in classification and machine learning.

Many machine learning algorithms use distance metrics to analyze the input data pattern to make any data-based decision. The most commonly used distance metric is the Euclidean distance due to its simplicity [8]. The Euclidean distance between signal  $A = (A_1, A_2, \dots, A_n)$  and  $B = (B_1, B_2, \dots, B_n)$ is defined as  $d_E(A, B) = \left[\sum_{i=1}^n (A_i - B_i)^2\right]^{1/2}$  [9]. To implement this function using silicon transistors, more than 20 transistors are needed per pixel to construct a subtracter circuit, an absoluter circuit, a squarer/divider circuit, and a square-rooter/multiplier circuit [10]–[12]. Considering a state-of-the-art smartphone camera with 12 million pixels, such a distance comparator circuit will need over 200 million

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

CMOS transistors. In this article, we propose to use dual-gate graphene transistors to calculate the Manhattan distance between signals. Here, the Manhattan distance between signal  $A = (A_1, A_2, \dots, A_n)$  and  $B = (B_1, B_2, \dots, B_n)$  is defined as  $d_M(A, B) = \sum_{i=1}^n |A_i - B_i|$  [13]. The use of graphene comparators endows the chip with great potential to increase the circuit density and speed.

To further reduce the energy consumption and latency, we propose to embed ferroelectric layers in the graphene transistors and integrate the memory and analog computing functions into one device, which can significantly reduce the energy and latency related to data transportation. To ensure the performance and reliability of the ferroelectric graphene transistors, a high-quality ferroelectric layer is a prerequisite. Traditionally, the ferroelectric materials are mainly based on complex perovskites, such as lead zirconate titanate (PZT), strontium bismuth tantalate (SBT), and lead magnesium niobate-lead titanate (PMN-PT), and these materials have been widely used in ferroelectric devices [14], [15]. However, these ferroelectric materials have a limitation in thickness scaling and are incompatible with CMOS processes. In the past few years, doped metal oxides, including hafnium oxide (HfO<sub>2</sub>) and zirconium oxide  $(ZrO_2)$ , were found to have ferroelectric phase [16]–[22]. Ferroelectric HfO<sub>2</sub> has the advantages of a high coercive field, excellent scalability (down to 1 nm), and good compatibility with CMOS processing [22]-[26]. In this article, we synthesized ultrathin hafnium zirconium oxide (HZO) with high remanent polarization and long retention time, which serves as an excellent storage layer in the graphene comparators.

Based on the prototype ferroelectric graphene comparators, we established the device model and simulated the functions of the graphene comparator arrays to illustrate their potential applications in image comparison, image classification, and motion detection. Note that these ferroelectric graphene transistors can process any analog signals that can be converted to voltages, including image pixel, sound, pressure, flow, temperature, and many other sensor inputs. These analog comparators will have broad applications in robotics, self-driving vehicles, security systems, and sensor networks.

## **II. EXPERIMENT**

## A. Device Design and Operating Principle

We propose a novel device structure: embedded-gate ferroelectric graphene transistor, as a basic building block for a comparator, illustrated in Fig. 2(a). The operating principle is as follows. The input voltage is applied to the top gate of the graphene transistor. A typical current voltage characteristic of a graphene transistor is illustrated in Fig. 2(b). The channel current, Iout, increases linearly with the absolute distance between the input voltage and the target Dirac voltage:  $|V_{\rm in} - V_{\rm Dirac}|$ . Here, the target Dirac voltage is determined by the polarization in the ferroelectric layer, which can be programmed by the pulses between the top and bottom gates, as illustrated in Fig. 2(c). An array of these graphene transistors can be used as a comparator to recognize an image as illustrated in Fig. 2(d) and (e). When the input image is the same as the target image, the total output current reaches a minimum. The value of the output current is a scalar



Fig. 2. Device structure and operating principles of the ferroelectric graphene transistor for analog comparison function. (a) Device structure. (b) I-V characteristics of the graphene transistor illustrating that the output current  $I_{out}$  is determined by the distance between input voltage and Dirac voltage  $|V_{in} - V_{Dirac}|$ . (c) Illustration of the drain current as a function of input voltage on the top gate in the graphene transistor with various polarizations in the ferroelectric HZO layer. (d) Illustration of graphene transistor array as comparator for image recognition. (e) Illustration of a target image and an input image in grayscale.

indicator of the degree of matching between the input image and the target image. In this way, each pixel will only need *one* graphene transistor. When compared with the traditional CMOS-based comparator, which needs more than 20 transistors per pixel [10]–[12], this graphene comparator circuit will consume a significantly smaller chip area and lower power. Using ferroelectric gate dielectrics in the graphene transistor, the information of the target image can be programmed and stored as the level of polarization in the ferroelectric HfO<sub>2</sub>. In this way, each graphene ferroelectric transistor will have both storage and analog processing dual function. This local storage of the target image will significantly reduce the power consumption and operation latency related to the data transfer.

#### B. Methods

Zr-doped HfO<sub>2</sub> (HZO) is deposited by alternating the Hf and Zr precursors with a 1:1 cycle ratio using an atomic layer deposition (ALD) tool. Thick (40 nm) Al<sub>2</sub>O<sub>3</sub> layer is deposited on the 12-nm HZO film for encapsulation. The HZO/Al<sub>2</sub>O<sub>3</sub> stacks are annealed in rapid thermal annealer (RTA) at 500 °C for 60 s to induce ferroelectric phase transformation. Then, the Al<sub>2</sub>O<sub>3</sub> layer is removed using hot phosphoric acid. For HZO capacitors, the top electrodes are formed on the HZO films and the remanent polarization is characterized using positiveup-negative-down (PUND) method. For the graphene/HZO transistors, after the RTA annealing, a window is patterned using lithography and the Al<sub>2</sub>O<sub>3</sub> layer is removed in the channel region. CVD graphene is transferred onto the exposed HZO in the channel region using the one-touch wet-transfer method [27]. Then, graphene is patterned by lithography and O<sub>2</sub> plasma. Source/drain contacts (Cr/Au) are formed using photolithography and ebeam deposition. The 2-nm Al is deposited on the graphene and then reoxidized to enhance the nucleation of the top gate dielectrics. Then, 20-nm  $Al_2O_3$ is deposited on top of the device using ALD. The top gate electrode (Cr/Au) is formed on the Al<sub>2</sub>O<sub>3</sub> layer. The dc I - V measurements and program tests are done in Lakethore cryogenic probe station using Keysight B-1500 analyzer. The PUND measurements are carried out using Keithley 4225-PMU.

(a)

(b)

Pulse Voltage (V)



10 15 20 2 Program Pulse Amplitude (V)

(c)

(d)

S

Voltage

Dirac

Time

(**A**1) 20

2

24 80K

\*\*\*\*\*\*\*\*\*\*\*

V<sub>TG</sub> (V)

(e)

Al<sub>2</sub>O<sub>3</sub>

Positive pulse  $\Pi$ 

TG

HZC

#### **III. RESULTS AND DISCUSSION**

# A. Tunable Polarization and Dirac Voltage in Ferroelectric Graphene FETs

High-quality ferroelectric HZO was synthesized using ALD. As shown in Fig. 3(a), the remanent polarization in HZO reaches 30  $\mu$ C/cm<sup>2</sup>, which serves as an important foundation for the ferroelectric graphene comparators. An Al<sub>2</sub>O<sub>3</sub> capping layer was deposited on the HZO layer before annealing to facilitate the ferroelectric phase formation in HZO. The remanent polarization of the HZO capacitor with the Al<sub>2</sub>O<sub>3</sub> capping layer is significantly higher than that without the Al<sub>2</sub>O<sub>3</sub> capping layer during annealing. The sacrificial Al<sub>2</sub>O<sub>3</sub> layer was removed after annealing to increase the vertical electric field in the HZO layer for a given gate pulse amplitude. As a result, the remanent polarization of the capacitor after Al<sub>2</sub>O<sub>3</sub> removal is much higher than that without Al<sub>2</sub>O<sub>3</sub> removal at a given voltage range. In addition, eliminating the nonferroelectric Al<sub>2</sub>O<sub>3</sub> layer also helps reduce the depolarization field and enhance the retention time of the polarization. The retention time of the polarization in ferroelectric HfO<sub>2</sub> can exceed ten years [28]. The ferroelectric HZO films with high remanent polarization and long retention can provide reliable and low power storage of the target signals, enabling the in-memory analog computing in these devices.

Dual-gate ferroelectric graphene transistors with 12-nm ferroelectric HZO were fabricated. Before programming, the transfer characteristics of the ferroelectric graphene transistor were measured. To eliminate the impact of the interface traps, the device was measured at low temperature (80 K). The Dirac voltage of the graphene transistor is close to zero, which is desired for the graphene comparator application, since both electron and hole branches are needed for the comparison function. The hysteresis is negligible, confirming that the interfacial trap effect is suppressed at this low temperature.

The tunability of the polarization in HZO and its impact on the Dirac voltage of the ferroelectric graphene transistor were studied using pulse measurements. The program pulses were applied on the top gate, while the silicon back gate is grounded. The vertical electric field between the top and bottom electrodes can control the polarization reversal in the HZO film effectively. Two pulse schemes were tested: opposite-polarity program pulses and preset-program pulses. In the opposite-polarity pulse scheme, a train of program pulses with alternating polarities and incremental amplitudes are applied between the top gate and the silicon bottom gate on the fresh devices, as illustrated in Fig. 3(b). The transfer curves of the graphene transistor before and after various program pulses are measured by sweeping the top gate voltage, as shown in Fig. 3(c). The extracted Dirac voltage is plotted as a function of program pulse amplitude [Fig. 3(d)]. When the pulse amplitude is below the coercive voltage, there are negligible shifts in the Dirac voltage after program pulses. When the pulse amplitude exceeds the coercive voltage, the Dirac voltage shifts to the positive (negative) direction after positive (negative) program pulses are applied. The higher the pulse amplitude, the larger the shift in Dirac voltage. The mechanism of this phenomenon is illustrated in Fig. 3(e). When a positive pulse is applied on the top gate, negative polarization charges are induced on the top surface of the HZO layer, which attract positive mobile charges in graphene. Therefore, the Dirac voltage shifts to the positive direction. The reverse is true for negative pulses. Note that in this pulse scheme, the polarization in HZO is a cumulative effect of all the pulses that have been applied on the device previously, since there is no reset or preset pulse in between the program pulses.

To quantify the effect of each individual program pulse on the polarization, a second pulse scheme is used, in which a preset pulse is applied before each program pulse, as illustrated in Fig. 4(a) and (c). In this case, the polarization of HZO is reset to a constant level before each program pulse, which ensures a fair comparison of the polarization switching induced by various program pulses. Fig. 4(b) shows the transfer curves of the graphene transistor after preset and program pulses. After a -24 V preset pulse is applied, the graphene transistor shows strong electron transport and the Dirac voltage is less than -3 V. After the positive program pulses with progressively increasing amplitude were applied on the gate, the Dirac voltage shifts monotonically to the positive direction, which is consistent with the mechanism illustrated in Fig. 4(d). The Dirac voltage is plotted as a function of pulse amplitude for both positive and negative program pulses, as shown in Fig. 4(e). We can see that positive pulses induce positive shifts and negative pulses induce negative shifts in Dirac voltage. Approximately, the Dirac voltage and the program



Fig. 4. Polarization and Dirac voltage of the graphene transistor tested using the preset-program pulses (the second pulse scheme). (a) and (c) Waveforms of the pulse train with positive and negative program pulses, respectively. A preset pulse is applied before each program pulse. The pulsewidth is 4 ms and the amplitude of the program pulse increases from 8 to 24 V. A fast  $I_{\rm D} - V_{\rm TG}$  sweep is taken after each program pulse to read the Dirac voltage. (b) and (d) Transfer characteristics of the graphene transistor after positive and negative program pulses, respectively. The  $I_{\rm D} - V_{\rm TG}$  transfer curves shift consistently with increasing pulse amplitude for both positive and negative pulses. (e) Extracted Dirac voltage as a function of program pulse amplitude for positive and negative program pulses. The Dirac voltages follow an approximate linear relationship with the pulse amplitude for both positive and negative program pulses. (f) Modeling of the transfer curves of the ferroelectric graphene transistor after positive program pulses. The symbols are the measured data and the lines are fittings. The channel width/length of the graphene transistor is 10  $\mu$ m/4  $\mu$ m and the drain voltage is 0.1 V.

pulse amplitude follow a linear relationship for both positive and negative pulses. Based on this correlation, we can convert the target Dirac voltages to the program pulse voltages, which will be essential for realizing the image comparison function. Note that after each preset pulse (-24 V), the transfer curve shifts back to nearly the same location [Fig. 4(b)], which means that these preset pulses provide reliable and consistent reset of the polarization. In addition, minimum conductance at the charge neutrality point is nearly unchanged when we vary the program pulse amplitudes, which will be an important feature for image processing, so that the current from all pixels can be equally weighted, regardless of the target voltage value. These results indicate that the ferroelectric graphene transistors can provide a promising hardware platform for image classification.

The transport of the ferroelectric graphene transistor is modeled using the following equation:

$$\sigma \approx \mu \sqrt{(en_{\text{Dirac}})^2 + C_{\text{TG}}^2 (V_{\text{TG}} - V_{\text{Dirac}})^2}$$
(1)

where  $\sigma$  is the conductivity of the graphene channel,  $n_{\text{Dirac}}$  is the carrier density at Dirac point,  $C_{\text{TG}}$  is the top gate capacitance,  $V_{\text{Dirac}}$  is the Dirac voltage,  $V_{\text{TG}}$  is the top gate voltage, and *e* is the electron charge. The graphene channel





Fig. 5. Potential application of graphene comparators (1): image comparison. The input and target image sizes are  $284 \times 177$  pixels. Case 1: the input image is the same as the target image. Case 2: the input image is similar to the target image. Case 3: the input image is very different from the target image. The corresponding total output currents for these three input images are 0.767, 0.779, and 0.844 mA, respectively. The output current serves as a scalar indicator of the similarity level between the input and target images. Low output current represents high similarity between two images. Here, we assume that the drain voltage is 1 mV and the channel width/length ratio is 1/4.

resistance is  $R_{ch} = l/\sigma W$ , where *l* and *W* are the length and width of the graphene channel, respectively. Considering the contact resistance  $R_c$ , the total resistance of the device can be expressed as  $R_{total} = R_{ch} + R_c$ . The drain current can be calculated from  $I_D = V_D/R_{total}$ , where  $V_D$  is the drain voltage. Fig. 4(f) shows the measured data and the modeled result. We can see that this model fits the experimental results very well. Based on this model, we can predict the drain current of the ferroelectric graphene transistor at any given input voltage  $V_{TG}$  for given Dirac voltage  $V_{Dirac}$ , that is, we can predict the output current for a given pair of input and target images, which will be discussed next.

## B. Potential Application of Graphene Classifier

1) Image Comparison: Image comparison is one of the essential processes in image analysis and artificial intelligence. Measures of the similarity between images play an important role in many image processing algorithms and applications including retrieval, classification, change detection, quality evaluation, and registration. Based on the device model established on the ferroelectric graphene transistor, we evaluated the potential of the ferroelectric graphene transistor arrays in image comparison application. Three input images with  $284 \times 177$  pixels are compared with the target image, as shown in Fig. 5. When the input image is the same as the target image (case 1), the top gate voltage is equal to the Dirac voltage at every graphene transistors in the array. The drain current reaches minimum at every transistor. As a result, the total output current reaches minimum  $I_{out_1}$  = 0.767 mA. If the input image is similar, but not identical, to the target image (case 2), then the top gate voltage will be slightly different from the Dirac voltage in some graphene transistors. Thus, the total output current will be slightly higher at  $I_{out 2} =$ 0.779 mA. If the input image is very different from the target image (case 3), then the output current is significantly higher than that in case 1:  $I_{out_3} = 0.844$  mA. We can see that the total output current can serve as a scalar indicator of the similarity between the input and output images. The higher the



Fig. 6. Potential application of graphene comparators (2): image classification. 10 000 training images and 500 test images in the MNIST data set are used in these tests. The KNN model is used for the classification operation. (a) Illustration of example training and test data images. (b) Accuracy as a function of training data size for graphene comparator and commercial comparators based on the Euclidean distance. (c) Accuracy as a function of *k* value with various training data sizes for graphene comparators.

similarity, the lower the total output current. Here, we assume the drain voltage is 1 mV and the channel width/length ratio is 4. Scaling down the drain voltage and width/length ratio can further reduce the output current and power consumption. The comparison function in these comparators is carried out in one step, which can be achieved at very high speed. Moreover, the image comparator based on graphene transistor only needs one transistor per pixel, which can significantly reduce the chip area. More importantly, the target image is stored in the comparator array using a ferroelectric layer, which is nonvolatile. This design can further reduce the energy consumption related to data storage and transportation. Furthermore, these graphene comparator arrays are especially suitable for large networks, where the output current from each transistor can be directly summed up. Regardless of the number of units in the array, the operation time remains constant, which will be very important for sensor network applications.

2) Image Classification: Image classification is a vital component in robotics, security systems, and image searching engines. A commonly used machine learning algorithm for image classification is the k-nearest neighbors (KNNs) algorithm. For each test image, the k-nearest training images are found, and the classification is decided by majority vote. In KNN, the critical step is to find the distance between two images. Traditionally, the distance between two images is calculated using the Euclidean method  $\sum_{k=1}^{MN} (A^k - B^k)^2$ . In this work, we conducted image classifications using graphene comparators. We used 10000 training images and 500 test images in the modified national institute of standards and technology (MNIST) data set to evaluate the accuracy of the graphene comparators and the conventional comparators based on the Euclidean distance. Fig. 6(a) shows some example training and test images. The classification accuracy is plotted as a function of training data size for these two types of comparators [Fig. 6(b)]. We can see that the accuracy of the



Fig. 7. Motion detection using graphene comparators. (a) Illustration of the motion detection operation using graphene comparator. The photodetector arrays detect the incoming images as a function of time. The graphene comparators compare these image frames with the reference image and generate output current. (b) Illustration of the change in the output current of the graphene comparators as a function of time. A change in the output current exceeding the threshold value constitutes motion detection. (c)  $\Delta I_{out}$  as a function of frame index for the test video. Here,  $\Delta I_{out} = I_{out}(n) - I_{out}(1)$ , where  $I_{out}(n)$  and  $I_{out}(1)$  are the output current for each image frame is simulated using the graphene comparator model, shown in Fig. 4.

graphene comparator is similar to or slightly better than that of the commercial comparator based on the Euclidean distance. Note that graphene comparators need many fewer transistors per pixel, which means that the chip size and complexity can be lower, when compared with the traditional comparator based on the Euclidean distance calculated digitally. Fig. 6(c)shows the accuracy as a function of k value with various training data size for graphene comparators. Here, k is the number of the nearest neighbors, which were used to vote. When the training data size is 200, the optimal k value is around 5. When the training data size exceeds 1000, the accuracy becomes insensitive to the k values in the range we tested here.

3) Motion Detection: Motion detection is very important in video surveillance systems and in navigation systems of self-driving cars, drones, and airplanes. Traditional motion detection involves data transmission from the sensors to the cloud and complex image processing using silicon CMOS circuits. In this project, we show that motion detection implemented using graphene comparators can be conducted locally in the sensors and the operation can be completed in one step. This ultrafast in-sensor motion detection will be critical in navigation systems. Fig. 7(a) illustrates the operation of motion detection using graphene comparators. The photodetector arrays capture the image frames as a function of time. Each frame is compared with the reference image, and an output current is generated based on the comparison. When a moving object appears in the frame, the total output current will increase immediately, as illustrated in Fig. 7(b). An appropriate threshold current change  $\Delta I_{\text{th}}$  is established, and any current change exceeding the threshold constitutes motion detection, which may trigger immediate action. The corresponding output current as a function of frame index

is shown in Fig. 7(c). Here, the change in the total output current is defined as  $\Delta I_{out} = I_{out}(n) - I_{out}(1)$ , where  $I_{out}(n)$ is the output current for the *n*th image frame, and  $I_{out}(1)$  is the output current for the first image frame. In this experiment, there is no moving object in the initial frame, which is taken as the reference image. We can see that when there is a person walking in front of the camera, the output current of the comparator array is significantly higher than that when only static background is in view. Since the graphene transistor can operate at very high speed, these graphene comparators will have great potential in ultrafast motion detection and in-sensor computing applications.

In addition, the absolute distance calculated by the ferroelectric graphene comparators can be used in regression analysis, compressed sensing, and frequency distribution. Furthermore, ferroelectric graphene comparators can be integrated with resistive random access memory (RRAM), phase change memory (PCRAM), ferroelectric tunneling junctions (FTJs), and spin transfer torque magnetic tunnel junctions (STT-MFJs) to form artificial neural networks for machine learning applications. Here, the devices with tunable conductance can serve as the synapses, while graphene comparators can calculate the residual errors and provide feedback to the synapses. These novel devices provide a new hardware platform for neuromorphic computing and machine learning.

## **IV. CONCLUSION**

In summary, we demonstrated that the ferroelectric graphene transistors can calculate the distance between two signals in the analog domain and store the reference signal in situ. Graphene's unique ambipolar characteristics and zero bandgap lead to the V-shaped transfer characteristics of the graphene transistor, which enable the direct calculation of the absolute distance between two signals. We synthesized ultrathin ferroelectric HZO with high remanent polarization ( $\sim 30 \ \mu C/cm^2$ ) and demonstrated ferroelectric graphene comparators with tunable Dirac voltages via ferroelectric polarization. Based on the characteristics of the prototype ferroelectric graphene comparators, we established a device model and simulated the functions of the graphene comparator arrays. Our results indicate that ferroelectric graphene comparator array can perform image comparison, image classification, and motion detection effectively. In these applications, each pixel only need one graphene transistor when compared with over 20 transistors per pixel in CMOS comparators, which creates a new alternative path to reduce the chip area, power consumption, and process latency. In addition, the nonvolatile nature of ferroelectric hafnium oxide will eliminate the need for frequent image loading/unloading, which will further reduce the power consumption related to the data transfer. These analog ferroelectric graphene comparators will have broad potential applications including navigation system in self-driving vehicles, robotic, security systems, and sensor networks.

#### REFERENCES

- B. G. Streetman and S. Banerjee, *Solid State Electronic Devices*, 7th ed. Boston, MA, USA: Pearson, 2015, p. 596.
- [2] R. S. Muller, T. I. Kamins, and M. Chan, Device Electronics for Integrated Circuits, 3rd ed. New York, NY, USA: Wiley, 2003, p. 528.

- [3] D. J. Perello, S. H. Chae, S. Song, and Y. H. Lee, "High-performance n-type black phosphorus transistors with type control via thickness and contact-metal engineering," *Nature Commun.*, vol. 6, no. 1, p. 7809, Jul. 2015.
- [4] A. V. Penumatcha, R. B. Salazar, and J. Appenzeller, "Analysing black phosphorus transistors using an analytic Schottky barrier MOSFET model," *Nature Commun.*, vol. 6, no. 1, p. 8948, Dec. 2015.
- [5] E. Wu *et al.*, "Dynamically controllable polarity modulation of MoTe<sub>2</sub> field-effect transistors through ultraviolet light and electrostatic activation," *Sci. Adv.*, vol. 5, no. 5, May 2019, Art. no. eaav3430.
- [6] Y.-F. Lin et al., "Ambipolar MoTe<sub>2</sub> Transistors and Their Applications in Logic Circuits," Adv. Mater., vol. 26, no. 20, pp. 3263–3269, 2014.
- [7] S. Larentis *et al.*, "Reconfigurable complementary monolayer MoTe<sub>2</sub> field-effect transistors for integrated circuits," *ACS Nano*, vol. 11, no. 5, pp. 4832–4839, May 2017.
- [8] T. Hastie, R. Tibshirani, and J. H. Friedman, *The Elements of Statistical Learning : Data Mining, Inference, and Prediction*, 2nd ed. New York, NY, USA: Springer, 2009, p. 745.
- [9] H. Anton, *Elementary Linear Algebra*, 10th ed. Hoboken, NJ, USA: Wiley, 2010, p. 568.
- [10] B.-D. Liu, C.-Y. Chen, and J.-Y. Tsao, "A modular current-mode classifier circuit for template matching application," *IEEE Trans. Circuits Syst. II. Analog Digit. Signal Process.*, vol. 47, no. 2, pp. 145–151, Feb. 2000.
- [11] T. Talaska, M. Kolasa, R. Dlugosz, and W. Pedrycz, "Analog programmable distance calculation circuit for winner takes all neural network realized in the CMOS technology," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 27, no. 3, pp. 661–673, Mar. 2016.
- [12] R. Długosz *et al.*, "Low power, low chip area, digital distance calculation circuit for self-organizing neural networks realized in the CMOS technology," *Solid State Phenomena*, vol. 199, pp. 247–252, 2013, doi: 10.4028/www.scientific.net/SSP.199.247.
- [13] P. E. Black and National Institute of Standards and Technology (U.S.), Dictionary of Algorithms and Data Structures. Accessed: Jun. 5, 2020. [Online]. Available: http://www.nist.gov/dads/
- [14] N. Setter *et al.*, "Ferroelectric thin films: Review of materials, properties, and applications," *J. Appl. Phys.*, vol. 100, no. 5, Sep. 2006, Art. no. 051606.
- [15] Y. Xu, Ferroelectric Materials and their Applications. Amsterdam, The Netherlands: Elsevier, 1991, pp. 1–391.
- [16] T. S. Böscke *et al.*, "Phase transitions in ferroelectric silicon doped hafnium oxide," *Appl. Phys. Lett.*, vol. 99, no. 11, Sep. 2011, Art. no. 112904.
- [17] X. S. N. Gong, H. Jiang, Q. Xia, and T. P. Ma, "Ferroelectricity of al-doped HfO<sub>2</sub>: Fast polarization switching, long retention and robust endurance," in *Proc. 46th IEEE Semiconductor Interface Spec. Conf.*, Arlington, VA, USA, 2015, pp. 1–5.
- [18] J. Müller et al., "Ferroelectricity in yttrium-doped hafnium oxide," J. Appl. Phys., vol. 110, no. 11, 2011, Art. no. 114113.
- [19] S. Mueller *et al.*, "Incipient ferroelectricity in al-doped HfO<sub>2</sub> thin films," *Adv. Funct. Mater.*, vol. 22, no. 11, pp. 2412–2417, Jun. 2012.
- [20] S. Mueller, C. Adelmann, A. Singh, S. Van Elshocht, U. Schroeder, and T. Mikolajick, "Ferroelectricity in Gd-Doped HfO<sub>2</sub> Thin Films," *ECS J. Solid State Sci. Technol.*, vol. 1, no. 6, pp. N123–N126, Jan. 2012.
- [21] T. Schenk *et al.*, "Strontium doped hafnium oxide thin films: Wide process window for ferroelectric memories," in *Proc. Solid-State Device Res. Conf. (ESSDERC)*, 2013, pp. 260–263.
- [22] J. Muller *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," in *IEDM Tech. Dig.*, Dec. 2013, pp. 8–10.
- [23] E. Yurchuk *et al.*, "Impact of scaling on the performance of HfO<sub>2</sub>-based ferroelectric field effect transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3699–3706, Nov. 2014.
- [24] U. Schroeder et al., "Hafnium oxide based CMOS compatible ferroelectric materials," ECS J. Solid State Sci. Technol., vol. 2, no. 4, pp. N69–N72, 2013.
- [25] A. Chernikova et al., "Ultrathin Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> ferroelectric films on Si," Acs Appl. Mater. Interface, vol. 8, no. 11, pp. 7232–7237, Mar. 23 2016.
- [26] S. S. Cheema *et al.*, "Enhanced ferroelectricity in ultrathin films grown directly on silicon," *Nature*, vol. 580, no. 7804, pp. 478–482, 2020.
  [27] C. Baeumer, S. P. Rogers, R. Xu, L. W. Martin, and M. Shim,
- [27] C. Baeumer, S. P. Rogers, R. Xu, L. W. Martin, and M. Shim, "Tunable carrier type and density in Graphene/PbZr<sub>0.2</sub>Ti<sub>0.8</sub>O<sub>3</sub> hybrid structures through ferroelectric switching," *Nano Lett.*, vol. 13, no. 4, pp. 1693–1698, Apr. 2013.
- [28] H. Ryu, K. Xu, J. Kim, S. Kang, J. Guo, and W. Zhu, "Exploring new metal electrodes for ferroelectric aluminum-doped hafnium oxide," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2359–2364, May 2019.