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Effect of dual gate control on the alternating current performance of graphene radio frequency device

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The excellent electrical properties of graphene, such as its high carrier mobility, gate tunability, and mechanical flexibility makes it a very promising material for radio frequency (RF) electronics. Here we study the impact of top and bottom gate control on the essential performance metrics of graphene RF transistors. We find that the maximum cut-off frequency improves as the bottom gate voltage is tuned towards the same polarity as the top gate bias voltage. These results can be explained by the bottom-gate tunable doping of the graphene underneath the metal contacts and in the under-lap region. These effects become more dramatic with device down-scaling. We also find that the minimum output conductance occurs, when the drain voltage roughly equals an effective gate voltage ($V_{eff} \approx V_{TG} + V_{BG} \cdot C_{BG}/C_{TG}$, where V_{TG} and V_{BG} are top and bottom gate voltage, C_{TG} and C_{BG} are the respective gate capacitance). The minimum output conductance is reduced as the bottom gate bias increases, due to the stronger control of the channel from the bottom gate, lessening the influence of the drain voltage on the drain current. As a result of these two influences, when the bottom gate voltage is tuned towards the same polarity as the top gate voltage, both the maximum oscillation frequency (f_{max}) and the intrinsic gain significantly improve. The intrinsic gain can increase as high as 3–4 times as the gain without the bottom gate bias. Tuning the bottom gate to enhance f_{max} and gain will be very important elements in the effort to enable graphene RF devices for practical use. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4816443]

I. INTRODUCTION

Graphene is a monolayer of carbon atoms arranged in a two-dimensional honeycomb lattice.[1] Interest in graphene for radio frequency (RF) applications stems mainly from its high intrinsic carrier mobility,[2,3] an attribute derived from its unique massless Dirac energy dispersion and weak electron-phonon coupling.[4] Recent demonstration of high cut-off frequency[5–8] and wafer-scale integrated circuits of graphene RF devices[9–11] represent technological promises, but challenges still remain. One outstanding challenge is the inability to obtain well-controlled current saturation in graphene RF devices,[6,12–14] an essential property for amplifier devices. Recent studies suggest that device electrostatics such as the channel potential profile and channel-contact interface play limiting roles on the drive current characteristic in graphene devices. This includes observations of quasi-saturation and negative differential resistance (NDR) behavior in graphene devices.[14,15] In this work, we perform a systematic study of performance metrics of graphene devices, including cut-off frequency, the output conductance, maximum oscillation frequency, and intrinsic gain. For the first time, the effect of a bottom gate bias on maximum oscillation frequency and intrinsic gain are reported. We find that when the bottom gate voltage is tuned towards the same polarity as the top gate voltage, the intrinsic gain increases significantly. This will provide an important path to enable graphene RF devices as competitive RF devices.

II. EXPERIMENT

The graphene was synthesized by the CVD method on copper foil. The detailed growth and transfer of the graphene was reported by Li *et al.*[16] After graphene formation, PMMA was spin-coated on top of the graphene layer formed on one side of Cu foil. This foil was then dissolved in a copper etchant. The resulting graphene/PMMA layer was transferred to a SiO_2/Si substrate, where the PMMA was later dissolved in acetone. The SiO_2 thickness was 280 nm. 20 nm Pd/30 nm Au stacks were used as the source/drain contacts. An AlO_x gate oxide was formed by oxidizing an Al layer that was deposited by electron-beam evaporation.[17] This was followed by the deposition of 15 nm of HfO_2 by atomic layer deposition (ALD). 1 nm Ti, 20 nm Pd, and 30 nm Au stacks were used as the gate electrodes. Fig. 1 shows a schematic of a graphene RF device on SiO_2/Si substrate. The RF device width was 20 μm and the length varied from 0.06 to 0.7 μm. The gate electrode is underlapped with the source/drain electrode. The gap between the source (drain) electrode and the gate electrode was 80 nm.

III. RESULTS AND DISCUSSION

A. Cut-off frequency

The RF characterization of the graphene devices was carried out using an Agilent B1500 parameter analyzer, an E8364C network analyzer, and 40 GHz microwave probes. The network analyzer was calibrated using a Short-Open-Load-Through (SOLT) method and a standard CS-5 substrate. On-chip "open" and "short" structures with exactly the same designs of the working devices were used to de-embed the parasitic effects. Fig. 2(a) shows a typical curve of current gain $|h_{21}|$ as a function of frequency. The cut-off frequency f_T is defined as the frequency at which the current gain $|h_{21}| = 1$. The cut-off frequencies were measured at

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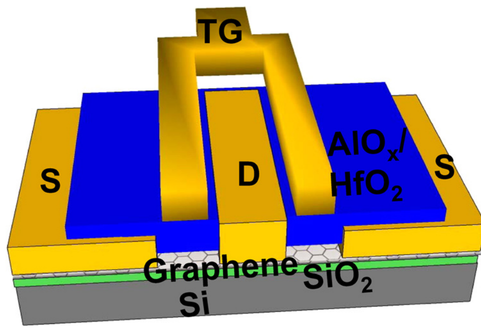

FIG. 1. Schematics of a graphene RF device on a SiO_2/Si substrate.

various top gate and bottom gate voltage combinations, as shown in Fig. 2(b). The same data were re-plotted as a function V_{TG}- V_{Dirac} at various V_{BG}, and are shown in Fig. 2(c). Notice, that when V_{BG} changes from -40 V to 40 V, the peak hole cut-off frequency reduces, while the peak electron cut-off frequency increases, at a given V_{TG}-V_{Dirac}. The peak cut-off frequency is plotted as a function of bottom gate voltage in Fig. 2(d). It is observed that f_T improves when V_{BG} is tuned towards the same polarity as V_{TG}. This is because the bottom gate changes the channel-contact junction from bipolar to unipolar and at the same time reduces the contact resistance and access resistance in the underlap region, hence reducing the overall device resistance. The asymmetry between the electron and hole f_T at zero bottom gate voltage is due to the initial p-doping caused by the large contact metal work function, which naturally favors a hole-dominated transport in the channel. In this hole-dominated channel case, tuning V_{BG} to be more negative increases the hole doping in graphene underneath the contact, hence reducing the contact resistance. In the electron transport dominated channel, the contact resistance is determined by the *pn* junction at the channel-contact interface instead, and depends on the details of the electrostatics such as the length of the *pn* transition region. These observations show that contacts and access resistance are playing a limiting role on the device trans-conductance or cut-off frequency.

We find these effects to be more pronounced upon device down-scaling. Figs. 3(a)–3(d) show the maximum f_T as a function of V_{BG} for gate lengths of 0.7, 0.4, 0.2, and 0.06μm, respectively. From these data, we extracted the relative changes in the maximum f_T at two different V_{BG} (i.e., $V_{BG} = 0$ and ± 10 V) as a function of the gate length, shown in Fig. 3(e). We can see that gate length down-scaling results in a larger V_{BG} modulation of f_T. This is consistent with our argument that f_T is series-resistance limited, since the device resistance is increasingly dominated by the series-resistance as the gate length is down-scaled.

B. Current saturation

In a silicon transistor, current saturation (i.e., g_D approaching zero) can be achieved under appropriate biasing. The large drain bias electrostatically depletes the drain side of

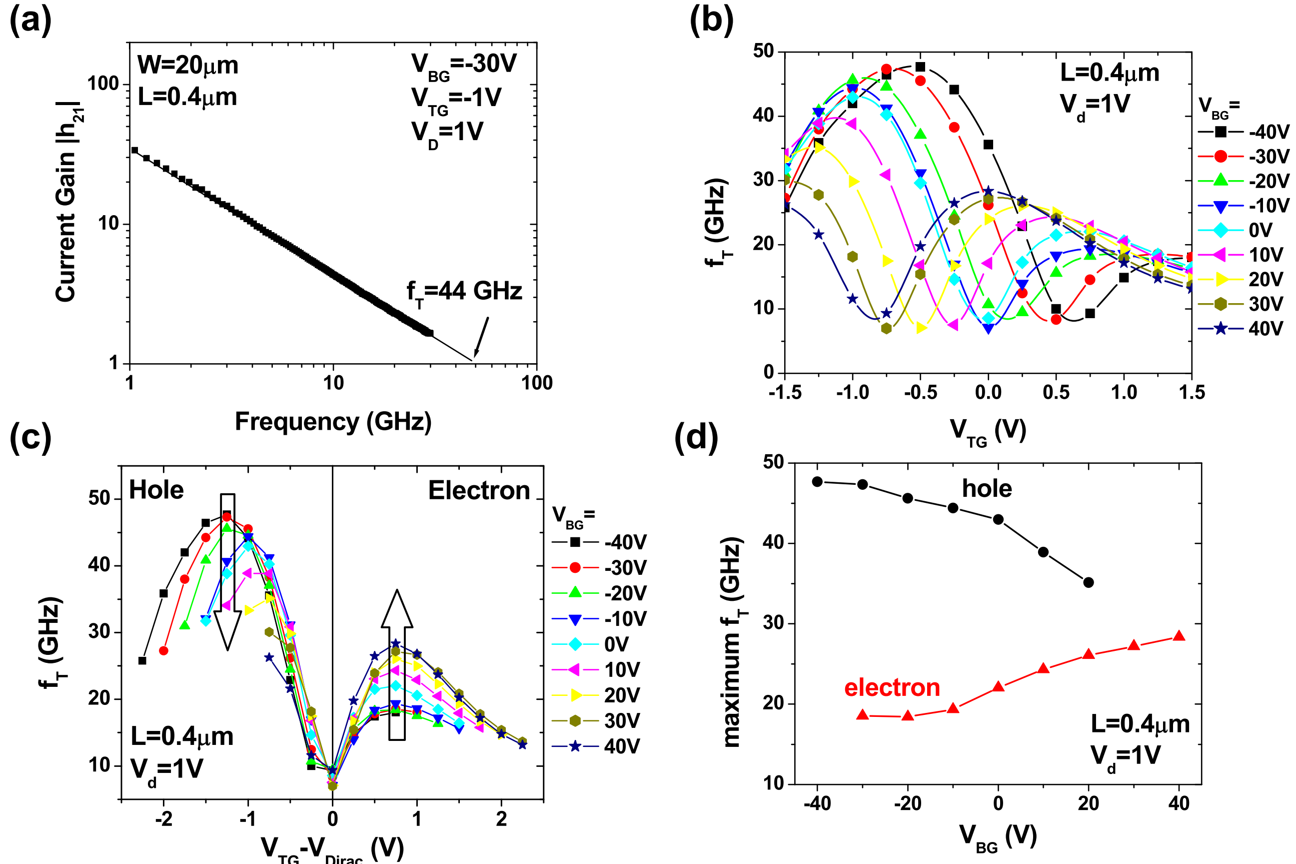

FIG. 2. (a) Current gain $|h_{21}|$ as a function of frequency in a graphene device with 0.4 μm gate length under -30 V bottom gate bias. (b) Cut-off frequency as a function of top gate voltage at various bottom-gate voltages. (c) Cut-off frequency as a function of $V_{TG} - V_{TG_Dirac}$ at various bottom-gate voltages. (d) Maximum cut-off frequency as function of bottom gate voltage for electron and hole transport.

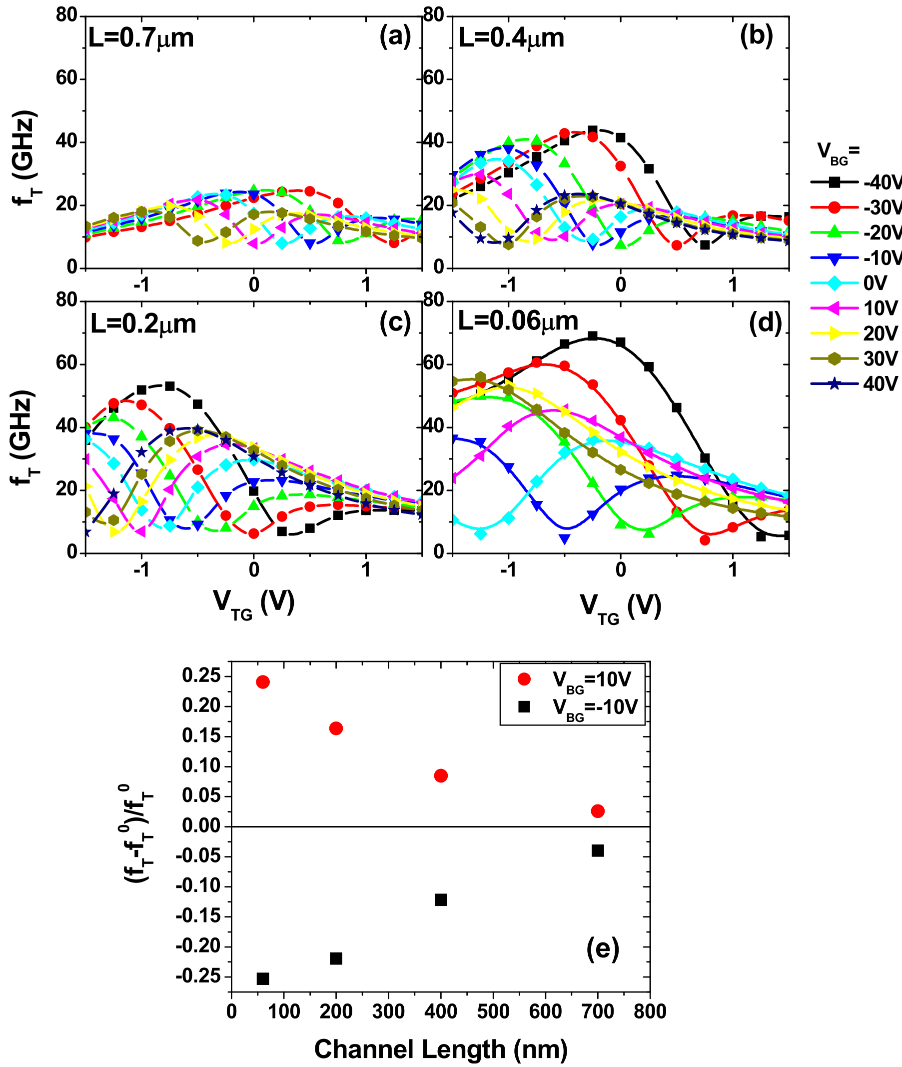

FIG. 3. (a)–(d) Cut-off frequency as a function of top-gate voltage at $V_D = 0.6\,\text{V}$ with various bottom-gate voltages for channel lengths of: (a) 0.7 μm, (b) 0.4 μm, (c) 0.2 μm, and (d) 0.06 μm. (e) Cut-off frequency percentage change as a function of channel length at V_{BG} voltages of 10 V and -10 V. f_T is the cut-off frequency at V_{BG} voltages of 10V or -10 V. f_T^0 is the cut-off frequency at $V_{BG} = 0\,\text{V}$.

inverted carriers, leading to the well-known pinch-off effect.[18] Due to the zero gap nature of graphene, such pinch-off effect is, strictly speaking, absent in this material. However, due to the vanishing density-of-states at the Dirac point, an analogous pinch-off effect can arise, albeit to a lesser degree. Indeed, quasi-saturation in the current characteristics of graphene devices has been observed and attributed to the quasi-Fermi level in the channel crossing the Dirac point.[13] More recently, an NDR effect was also observed and explained within the same physical picture.[14,15] Theory suggests that the contacts might also produce similar effects.[19] The dual-gated transistor structure used in this study allows us to separate the effect of channel and contacts on the device performance. The insets of Figs. 4(a) and 4(b) show the drain current as a function of the drain voltage at various bottom gate voltages with $V_{TG} = 0.5\,\text{V}$ and $V_{TG} = -0.5\,\text{V}$, respectively.

Both the top and bottom gates control the channel electrostatics in the device. The total charge induced is $Q_{total} = C_{TG}V_{TG} + V_{BG}C_{BG}$. The ratio between C_{BG} and C_{TG} can be extracted from the plot of top gate Dirac voltage as a function of bottom gate voltage, shown in Fig. 4(c). Here we get $C_{BG}/C_{TG} = 0.028$. Since $C_{TG} \gg C_{BG}$, i.e., the "total channel capacitance" is dominated by C_{TG}, we can define an effective gate voltage on the graphene channel

$$V_{eff} = Q_{total}/C_{total} \approx V_{TG} + V_{BG} \cdot C_{BG}/C_{TG}. \qquad (1)$$

This effective gate voltage, V_{eff}, is simply the effective channel doping due to the combined dual gating. Relating the charge to voltage would be convenient in the subsequent discussion. It is also known that the doping of graphene underneath the metal contacts can be modulated by the bottom gate V_{BG}, which modifies the channel-contact resistances due to the presence of an electrostatic junction.[20–28] Hence, by studying how g_m and g_D varies with V_{eff} and V_{BG}, we can gain insights into how the various device performance metrics are related to the channel and contact electrostatics.

The corresponding device output conductance $g_D = dI_D/dV_D$ as a function of V_D is plotted in Figs. 4(a) and 4(b) for electron and hole dominated transport, respectively. At different combinations of V_{TG} and V_{BG}, a minimum output conductance is observed, which occurs at different V_D, herein denoted as $V_{D,min}$. The inset of Fig. 4(d) plots $V_{D,min}$ as function of V_{BG}, and Fig. 4(d) plots $V_{D,min}$ as a function of V_{eff}. In the latter, both the electron and hole curves overlap one another. This suggests that the mechanism for minimum device output conductance is channel-dominated, rather than contact-dominated. The fitting shown in Fig. 4(d) indicates that the device minimum output conductance occurs when

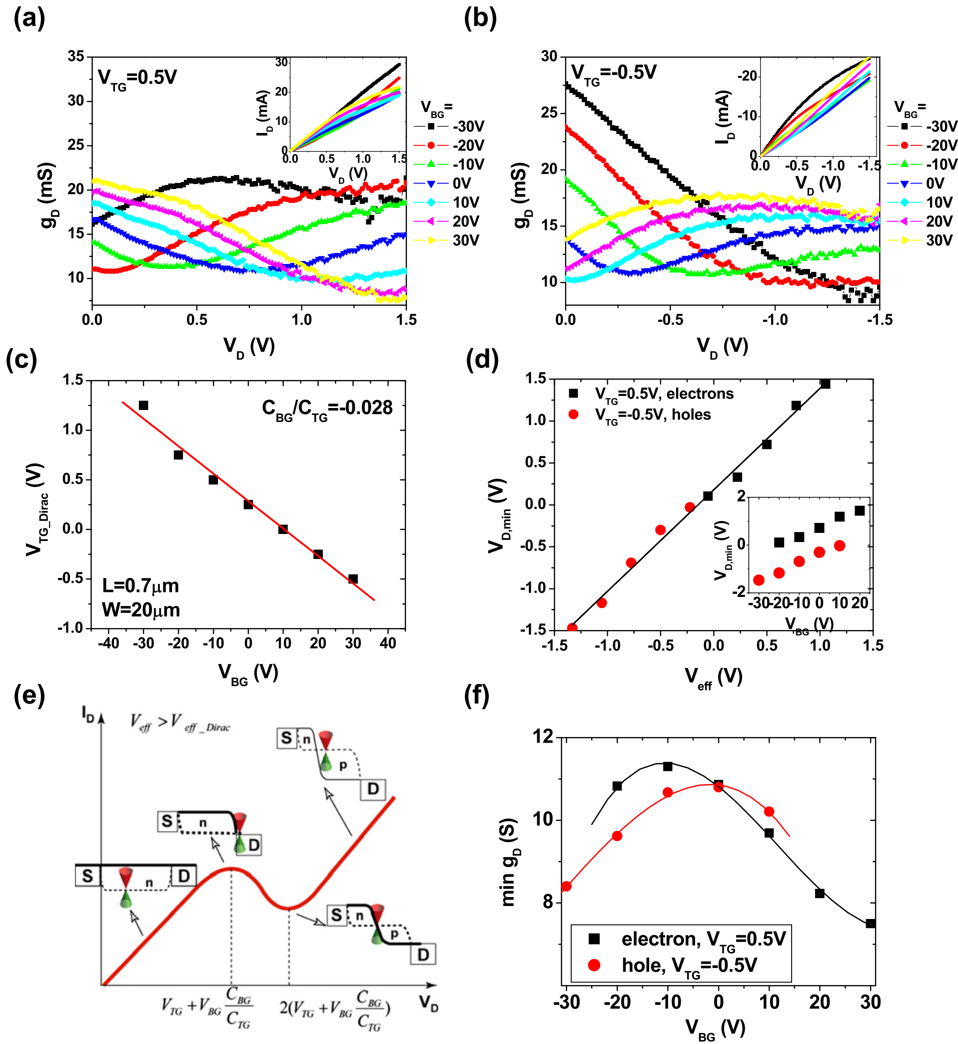

FIG. 4. (a) Output conductance g_D as a function of drain voltage at $V_{TG} = 0.5\,V$ for graphene RF device with channel length of $0.7\mu m$. The inset shows the drain current as a function of drain voltage at $V_{TG} = 0.5\,V$. (b) Output conductance g_d as a function of drain voltage at $V_{TG} = -0.5\,V$ for graphene RF device with channel length of $0.7\mu m$. The inset shows the drain current as a function of drain voltage at $V_{TG} = -0.5\,V$. (c) Top gate Dirac voltage as a function of the bottom gate voltage. From this plot, $C_{BG}/C_{TG} = 0.028$ is extracted. (d) Drain voltage at minimum output conductance $V_{D,min}$ as a function of V_{eff}. The inset shows the drain voltage at minimum output conductance $V_{D,min}$ as a function of bottom gate voltage. The symbols are measured data and the line is the linear fitting for both electron and hole data sets. (e) Illustration of drain current as a function of drain voltage. The inset shows the band diagram of the graphene channel at a constant total effective gate voltage ($V_{eff} > V_{eff_Dirac}$, i.e., electrons) at different drain biases $V_D = 0\,V$, $V_D = V_{eff}$, $V_D = 2V_{eff}$, and $V_D > 2V_{eff}$. The solid lines represent the local Fermi energy along the channel and the dashed lines represent the position of the local Dirac point in the graphene band structure. (f) Minimum output conductance as a function of bottom gate voltage at $V_{TG} = 0.5\,V$ and $V_{TG} = -0.5\,V$.

$V_D \approx 1.2\,V_{eff}$. We explain this behavior in terms of the channel electrostatics below.

Fig. 4(e) illustrates the drain current as a function of drain voltage and energy band diagram of the graphene channel for different drain voltages V_D. In the limit where $V_D \approx 0$, the channel electrostatics is mainly controlled by the gate, with the dominant carrier being electrons. Here, the channel behaves like an ohmic resistor where current increases linearly with V_D. When $V_D \approx V_{eff}$, the graphene at the drain contact reaches charge neutrality, and the channel resistance is dominated by this maximum local resistance. With increasing V_D, the charge neutrality point migrates deeper into the channel. This results in a roll-off of the drain current. This trend continues until $V_D > 2\,V_{eff}$, where the channel doping becomes inverted from electron- to hole-dominated transport with the charge neutrality point passing the middle of the channel. Thereafter, the drain current begins to increase again. This line of reasoning explains the observed behavior shown in Fig. 4(d), i.e., that the minimum g_D occurs when V_D is between V_{eff} and $2V_{eff}$.

The minimum g_D as a function of bottom-gate voltage is plotted in Fig. 4(f). It is observed that the minimum g_D substantially improves when $|V_{BG} - V_{BG_Dirac}|$ increases. This is because that, as the $|V_{BG} - V_{BG_Dirac}|$ increases, the bottom gate gains more control on the device, and as a result, the drain current is less influenced by the drain voltage giving a lower minimum output conductance.

Note the minimum output conductance g_D is positive in these cases, due to the low gate voltage used for these measurement ($V_{TG} = \pm 0.5\,V$ and $V_{BG} = -30\,V \sim +30\,V$), so that the minimum output conductance can be observed in relatively low drain voltage range to avoid stressing the device during measurement. Similar to the case of single gate devices,[15] we can derive that for a given ratio of $\sigma_{\min}/C_{total}\mu$ (where $\sigma_{\min}$ is minimum conductivity, C_{total} is the total capacitance per unit area, and μ is the channel mobility), the total gate voltage $\tilde{V}_{GS} = V_{eff} - V_{eff_Dirac}$ needs to be larger than $\sqrt{8}\sigma_{\min}/C_G\mu$ so that negative differential resistance can develop. Typically, the thinner the gate dielectric and the lower the charge impurities in the substrate, the lower the $\sigma_{\min}/C_{total}\mu$ value and consequently the wider the operating window for negative differential resistance.

C. Maximum oscillation frequency and intrinsic gain

The maximum oscillation frequency f_{max} of the device was also investigated. Fig. 5(a) shows typical results on the maximum available gain (MAG) as a function of frequency in a graphene device with $0.4\,\mu m$ gate length under $-30\,V$ bottom gate bias. The maximum oscillation frequency f_{max}

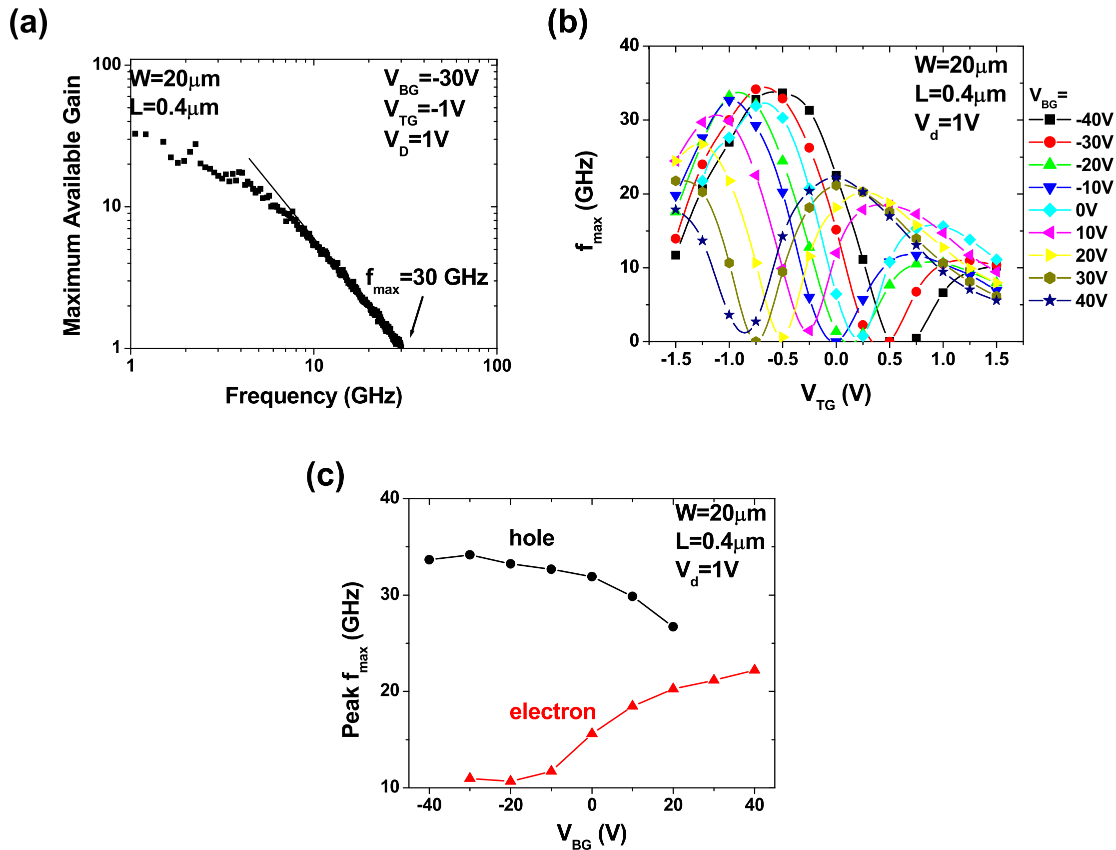

FIG. 5. (a) MAG as a function of frequency of a graphene device with 0.4 μm gate length under -30 V bottom gate bias. A maximum oscillation frequency f_{max} of 30 GHz is extracted from this plot. (b) f_{max} as a function of top gate voltage at various bottom-gate voltages. (c) Peak f_{max} as a function of bottom gate voltage for electrons and holes.

is obtained when $MAG = 1$. Fig. 5(b) shows f_{max} as a function of top gate voltage at various bottom gate voltages. The peak f_{max} as a function of bottom gate voltage is summarized in Fig. 5(c). Similar to the cut-off frequency f_T, the f_{max} also improves, when V_{BG} is tuned towards the same polarity as V_{TG}. The $f_{\max}$ is given by $f_{\max} \approx f_T/\sqrt{4g_D(R_s+R_G)+8\pi C_g R_G f_T}$, where R_s is the series resistance, R_G is the gate resistance, C_g is the gate capacitance, and $g_D = dI_D/dV_D$ is the output conductance. Therefore, when V_{BG} is tuned towards the same polarity as V_{TG}, f_T increases while g_D decreases, resulting in the increase of f_{max}.

The intrinsic gain is another important figure-of-merit for RF device. It is defined as *intrinsic gain* $= |g_m/g_D|$, where g_m and g_D are the trans-conductance and output conductance, respectively. They are defined as $g_m = dI_D/dV_G$ and $g_D = dI_D/dV_D$, where I_D is the drain current, V_G and V_D are the gate and drain voltages. Fig. 6(a) shows the intrinsic gain as a function of top gate voltage at various bottom gate voltages. The peak gain as a function of bottom gate voltage is

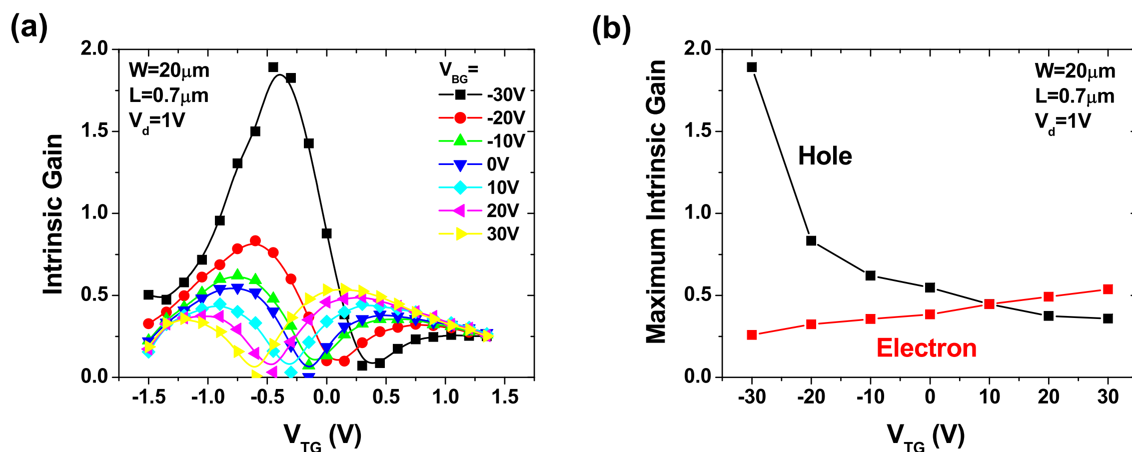

FIG. 6. (a) Intrinsic gain as a function of top gate voltage at various bottom-gate voltages in a graphene device with gate length of 0.7μm. (b) Maximum intrinsic gain as a function of bottom gate voltage for electrons and holes.

summarized in Fig. 6(b). We can see that the intrinsic gain increases dramatically as the bottom gate voltage is tuned towards the same polarity as V_{TG}. In particular, when the bottom gate voltage decreases from zero to $-30\,V$, the intrinsic gain increases from 0.55 to 1.90, i.e., the intrinsic gain at $V_{BG} = -30\,V$ is 3–4 times as high as the intrinsic gain at $V_{BG} = 0\,V$. This is because that, when V_{BG} is tuned towards the same polarity as V_{TG}, g_m increases while g_D decreases which results in a significant increment of intrinsic gain.

Since graphene is a zero band-gap material that has no device pinch-off, achieving high intrinsic gain and high f_{max} has been a challenging problem.[12,29] Tuning the bottom gate bias provides a way to boost intrinsic gain and f_{max}.

IV. CONCLUSION

In summary, we find that a proper balance of the top gate and bottom gate biases in a dual gate structure can significantly influence the RF device performance. Tuning the doping of graphene underneath the metal contacts and in the under-lap region by a bottom gate can enhance or degrade the cut-off frequency dramatically, especially in the case of channel down-scaled devices. Percentage wise the maximum cut-off frequency increases more than ten times when the channel length is scaled down from 0.7 to 0.06μm. The current saturation, however, depends on the total effective gate voltage produced by the top and bottom gate bias. When the drain voltage is comparable to the total effective gate voltage, the output transconductance reaches a minimum. The minimum output conductance is reduced as the bottom gate bias increases, due to the stronger control of the channel from the bottom gate, which lessens the influence of the drain voltage on the drain current. When the bottom gate voltage is tuned towards the same polarity as the top gate voltage, the maximum oscillation frequency (f_{max}) and intrinsic gain significantly improve. The intrinsic gain can become 3–4 times as high as the gain without a bottom gate bias. Bottom gate tuning to enhance the f_{max} and gain will be a very important element to enable graphene devices to be of practical use.

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