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Dielectric-induced interface states in black phosphorus and tungsten diselenide capacitors

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The interfaces between two-dimensional (2D) materials and gate dielectrics play an important role in the performance and reliability of 2D electronic devices. In this work, we systematically studied the capacitance and interface states of a narrow bandgap material (black phosphorus, BP) and an intermediate bandgap material (tungsten diselenide, WSe_2). We found that their capacitance–voltage (CV) characteristics are drastically different. The BP capacitor CVs demonstrate ambipolar and low-frequency properties, while WSe_2 capacitor CVs shows unipolar (p-type) and high-frequency behavior. The narrow bandgap of BP ($\sim$0.3 eV) enables large amounts of minority carriers, low generation-recombination resistance, and short minority carrier lifetime, giving low-frequency behavior of the CVs, while the wide bandgap of WSe_2 ($\sim$1.21 eV) leads to the high-frequency behavior of the CVs. The nearly intrinsic (low) doping of the BP flake results in ambipolar CVs which are symmetric about the midgap. The naturally p-type doping in WSe_2 gives unipolar CVs similar to p-type silicon. In both materials, the interface state density is as high as $10^{13}\,cm^{-2}eV^{-1}$. Although 2D materials are free of dangling bonds, their intimate contact with high-k dielectrics like Al_2O_3 could generate a larger number of interface states and degrades the device performance. Hexagonal boron nitride (hBN) effectively reduces the interface state density as dielectrics. The interface state for BP/hBN capacitor shows much lower density than counterpart with Al_2O_3 gate dielectric. We also found that the interface state density increases exponentially with the gate voltage when the surface Fermi level is swept from the midgap toward the band edge. *Published by AIP Publishing.*
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Interface traps are electrically active defects located at the interface between gate dielectric and semiconductors. Interface traps have energy levels within the forbidden gaps of the semiconductors. They are distributed with density, $D_{it} \equiv \partial N_{it}/\partial E$, in units of $cm^{-2}eV^{-1}$, where N_{it} is the number of interface traps per unit area and E is energy. Interface states are capable of trapping and de-trapping charge carriers and can have an adverse effect on device performance. In metal oxide field-effect transistors (MOSFETs), the charged interface traps can reduce the carrier mobility by Coulomb scattering and thus reduce the drain current. The interface trap capacitance can degrade the subthreshold swing and reduce the on/off current ratio for a given supply voltage. In tunneling field-effect transistors (TFETs), the interface states can induce trap-assistant tunneling in the "off" states, which will increase the off-current and degrade the subthreshold swing. In Esaki diodes and resonant tunneling diodes (RTDs), the interface states can introduce additional valley currents, which will reduce the peak-to-valley current ratio and make it difficult to observe negative-differential resistance (NDR) effect at room temperature.[1]

For electronic devices based on 2D materials, their performance and reliability are even more sensitive to the interface quality, since 2D materials have thin bodies and extremely large surface-to-body ratio. To ensure the technologies based on 2D materials are predictable, reliable, and stable, it is very important to characterize and monitor the quality of the interface between 2D materials and gate dielectric/substrate. Among the large variety of 2D materials, black phosphorus (BP) and WSe_2 are two promising candidates for electronic and photonic devices. Black phosphorus has a puckered hexagonal structure and anisotropic in-plane electrical and optical properties.[2–6] The bandgap of black phosphorus is direct and tunable from 0.3 eV (bulk) to 1.4 eV (monolayer).[4,7–11] The transistors based on black phosphorus show high carrier mobility (up to 5200 $cm^2V^{-1}s^{-1}$ at room temperature and $\sim$45000 $cm^2V^{-1}s^{-1}$ at 2 K) and good on/off ratio ($\sim10^5$).[3,12–24] WSe_2 is an important member of the transition metal dichalcogenide (TMD) family due to its smaller effective electron and hole masses compared to most of the other TMDs.[25,26] The small effective mass implies high carrier mobilities. The hole mobility of WSe_2 is reported to reach 500 $cm^2V^{-1}s^{-1}$ at room temperature and 2.1×10^3 $cm^2V^{-1}s^{-1}$ at 5 K.[27,28] Various electronic and photonic devices based on black phosphorus and WSe_2—including metal-oxide field-effect transistors (MOSFETs), tunneling devices, bipolar transistors, photodetectors, light emitting diodes, and solar cells—have been demonstrated.[13–23,26,27,29–42] However, there is very limited research on the interface properties between these 2D materials and gate dielectrics/substrates. In this paper, we systematically study the interface states of black phosphorus and WSe_2 using capacitance and conductance methods. We found that the capacitance–voltage (CV) characteristics of black phosphorus and WSe_2 capacitors are dramatically different due to the different sizes of the bandgaps. In addition, we found the interface state density increases exponentially with gate voltage, when the capacitor is biased from midgap towards band edge.

The metal-insulator-semiconductor-metal (MISM) capacitors based on black phosphorus and WSe_2 were fabricated on quartz substrates to eliminate the potential parasitic capacitances between the probe pads and the substrates. Embedded metal electrodes (30 nm Ti/20 nm Au) were formed by photo-lithography, e-beam metal evaporation, and lift-off. The black phosphorus and WSe_2 flakes were exfoliated from bulk crystals and stacked onto the bottom metal electrodes by aligned dry transfer.[43] Al_2O_3 was deposited as gate dielectric using atomic layer deposition (ALD) at 200 °C.[44] The top electrodes were formed by photo-lithography, metal deposition and lift-off. The Al_2O_3 at the pad area of the bottom electrodes was removed using hot phosphoric acid in order to ensure good contacts. The structure of the MISM capacitor is illustrated in Fig. 1(a). Al_2O_3 thickness is ~30 nm measured by profilometer on a control structure. The capacitors were measured in vacuum at various temperatures using a Lakeshore cryogenic probe-station. The capacitance and conductance of the capacitors were measured at various frequencies using a Keysight parameter analyzer. The equivalent circuit model of the device, simplified parallel model of the device and measurement model in parallel mode are illustrated in Fig. 1(b).

The capacitances of the WSe_2 and black phosphorus capacitors were measured as a function of gate voltage at various frequencies, shown in Figs. 2(a) and 2(b), respectively. Here, the capacitance of the device, C_m, is normalized with respect to the gate dielectric capacitance, C_{ox}. The thickness of the WSe_2 is ~30 nm and the thickness of the black phosphorus is ~55 nm. The gate dielectrics in both capacitors are Al_2O_3 grown by ALD with thickness of ~30 nm. These two sets of CVs are drastically different. The CVs of the WSe_2 capacitor are unipolar and high-frequency-like, while the CVs of the black phosphorus capacitor are ambipolar and low-frequency-like. The CV curves of black phosphorus capacitor are nearly symmetric about the minimum capacitance point at gate voltage of ~0.4 V. Even at a very high frequency (2.5 MHz), the CV shows low-frequency behavior, i.e., the capacitance at inversion is nearly as high as the capacitance level at accumulation. These phenomena can be attributed to the narrow bandgap and low doping of the black phosphorus flake. The thickness of this black phosphorus flake is ~55 nm, which corresponds to a ~0.3 eV bandgap.

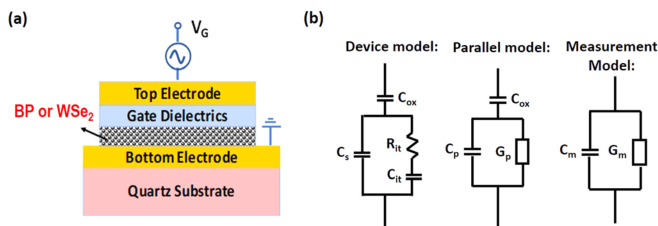

FIG. 1. (a) Illustration of the MISM capacitor structure on quartz substrate. (b) The equivalent circuit model of the device, simplified parallel model of the device, and the measurement model in parallel mode. C_{ox} is the gate dielectric capacitance, C_s is the semiconductor capacitance, C_{it} is the interface trap capacitance, and R_{it} is the resistance due to interface traps. C_p and G_p are the extracted parallel capacitance and conductance, respectively. C_m and G_m are the measured capacitance and conductance in parallel mode, respectively.

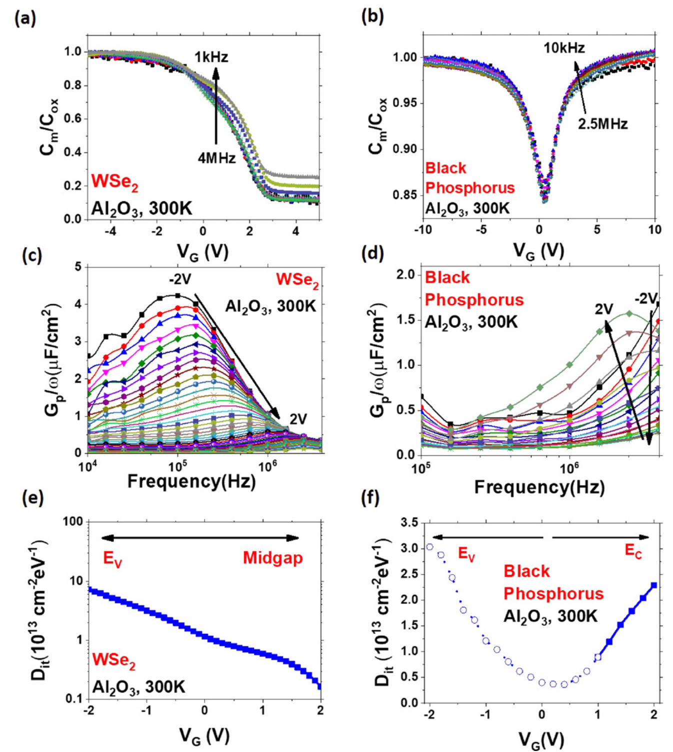

FIG. 2. The interface states of WSe_2 and black phosphorus capacitors with Al_2O_3 gate dielectrics at 300 K. (a) Capacitance as function of gate voltage of a WSe_2 capacitor measured at various frequencies. (b) Capacitance as function of gate voltage of a black phosphorus capacitor measured at various frequencies. (c) G_p/ω as a function of frequency of the WSe_2 capacitor measured at various gate voltages. (d) G_p/ω as a function of frequency of the black phosphorus capacitor measured at various gate voltages. (e) Interface state density, D_{it}, as function of gate voltage extracted from the G_p/ω plot for the WSe_2 capacitor. (f) Interface state density, D_{it}, as function of gate voltage extracted from the G_p/ω plot for the black phosphorus capacitor. Hollow dots indicate estimations from incomplete G_p/ω curves without peaks.

The narrow bandgap of black phosphorus leads to a large number of minority carriers generated thermally at room temperature, which can effectively reduce the generation/recombination resistance of the minority carriers, R_{gr}, and consequently reduce the minority carrier time constant, $\tau_R = R_{gr}C_D$, where C_D is depletion capacitance. Therefore, at room temperature, the minority carriers can still follow the AC signal and the CVs show low-frequency behavior, even when the testing frequency is in MHz regime. The very low doping in black phosphorus flakes yields symmetric CVs about the midgap. These two factors result in the nearly V-shaped CVs. For WSe_2, however, the bandgap is much larger (~1.21 eV), there are very few minority carriers generated at room temperature and the minority carrier time constant is very long. Therefore, the minority carriers cannot follow the AC signal and the CVs show high-frequency behavior, even when the measurement frequency is as low as 1 kHz. In addition, the exfoliated WSe_2 flake is naturally p-type doped, which gives the unipolar CVs, similar to p-type silicon. These results indicate that we can use the CV characteristics to evaluate the bandgap of the 2D materials. At a given temperature and testing frequency, the wider the bandgap of the semiconductor, the stronger the high-frequency behavior in the CV characteristics.

To evaluate the interface state density quantitatively, we extracted the parallel conductance from the capacitance and conductance measurements. As shown in Fig. 1(b), the parallel conductance, G_p, can be extracted from the measured capacitance, C_m, and conductance, G_m, by the following equation:[45]

$$G_p = \frac{\omega^2 G_m {C_{ox}}^2}{{G_m}^2 + \omega^2 (C_{ox} - C_m)^2}, \quad (1)$$

where ω is the measurement frequency and C_{ox} is the oxide capacitance. Figures 2(c) and 2(d) show the G_p/ω plot at various gate voltages for black phosphorus and WSe_2 capacitors, respectively.

The relation between G_p/ω and the interface state density D_{it} is given by[45]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})\right]^2, \quad (2)$$

from which one can deduce the interface state density, D_{it}, and the respective time constant, τ_{it}, from the following relations:[45]

$$D_{it} = \frac{2.5}{e}\left(\frac{G_p}{\omega}\right)_{peak}, \quad (3)$$

$$\tau_{it} = \frac{1.98}{2\pi f_0}. \quad (4)$$

Here, $(G_p/\omega)_{peak}$ is the maximum G_p/ω value and f_0 is the frequency at which this maximum G_p/ω is obtained. The extracted interface state densities, D_{it}, are plotted as a function of gate voltages for WSe_2 and black phosphorus, shown in Figs. 2(e) and 2(f), respectively. We can see that the interface state densities decrease exponentially with increasing gate voltage towards the midgap for the WSe_2 capacitor. This exponential dependence of the interface state density on gate voltage is similar to what has been observed in silicon. In silicon, the D_{it} distribution is typically modeled using this equation: $D_{it} = D_{it0} e^{\phi_s/\phi_{s0}}$, where D_{it0} is the interface trap density at the midgap, ϕ_s is the surface potential measured from the intrinsic Fermi level, and ϕ_{s0} is a characteristic potential, which describes the slope of D_{it} near the band edges. Note that $\phi_s = E_{Fs} - E_i$, where E_{Fs} is the Fermi level at the interface between the semiconductor and gate dielectrics and E_i is the intrinsic Fermi level of the semiconductor. As the surface Fermi level, E_{Fs}, is moving from the midgap towards the band edge, the interface state density increases exponentially, as we observed in the WSe_2 capacitor. For the black phosphorus capacitor, the interface state density first decreases, then increases, with the increasing gate voltage. The interface state density reaches minimum, when the gate voltage is ~0.4 V, which corresponds to the minimum capacitance in the CVs, shown in Fig. 2(b). At this gate voltage, the surface Fermi level reaches midgap. As the surface Fermi level is swept from midgap to the conduction/valence band edges, the interface state density increases exponentially. The very low doping and the narrow bandgap of the black phosphorus make it possible to observe the interface states in both the upper and lower halves of the bandgap.

The temperature dependence of the capacitance and the interface states were also studied. Figure 3(a) shows the CVs of a black phosphorus capacitor measured at various temperatures from 6 K to 300 K. The testing frequency is 2.5 MHz. As the temperature decreases, the inversion capacitance of the black phosphorus capacitor decreases and the CV characteristics migrate from low-frequency to intermediate-frequency behavior. The reason for this is that, as the temperature decreases, the generation-recombination rate in black phosphorus decreases, and as a result the generation-recombination resistance, R_{gr}, increases and the minority carrier response time, τ_R, increases. Therefore, as the temperature decreases, the minority carriers follow the AC signal less readily, and the CVs gradually change from low-frequency to high-frequency behavior for a given testing frequency. From the measured capacitance and conductance, we can extract the G_p/ω as a function of frequency at various gate voltages [Fig. 3(b)] and at various temperatures [Fig. 3(c)]. As the temperature increases, the G_p/ω peak shifts to higher frequencies. The extracted interface state density, D_{it}, was plotted as a function of temperature, shown in Fig. 3(d). We can see that the interface state density is not strongly dependent on temperature for our samples.

The interface states are not only dependent on the 2D materials, but also influenced by the gate dielectrics, which are in intimate contact with the 2D materials. The CVs and the G_p/ω plots of black phosphorus capacitors with hexagonal boron nitride (hBN) are shown in Figs. 4(a) and 4(b). Comparing Fig. 4(b) to Fig. 2(d), we can see that the peak height of the G_p/ω plots for the capacitor with Al_2O_3 is much higher than that with hBN. Consequently, the extracted interface state densities, D_{it}, for capacitor with Al_2O_3 are much higher than that with hBN, shown in Figs. 2(f) and 4(c), respectively. Previously, it has been reported that the surface roughness in crystalline hBN is much smaller than that in SiO_2, and this low interface state density in hBN provides another advantage to using hBN as gate dielectrics.

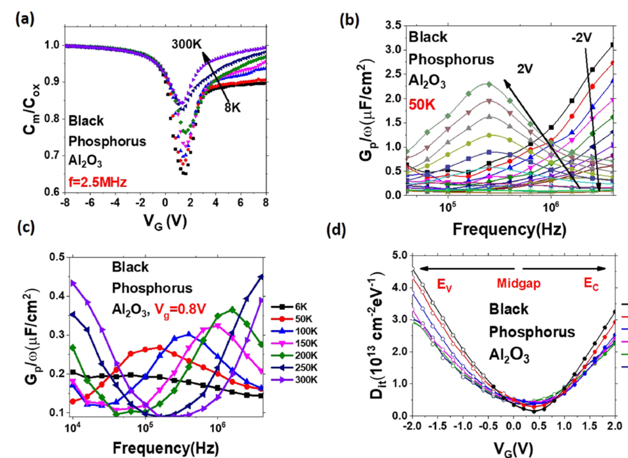

FIG. 3. Temperature dependence of interface states in black phosphorus capacitors with Al_2O_3 gate dielectrics. (a) Capacitance as a function of gate voltages measured at various temperatures. The measurement frequency is 2.5 MHz. (b) G_p/ω as a function of frequency measured with various gate biases at 100 K. (c) G_p/ω as a function of frequency at various temperatures. The gate bias is 0.8 V. (d) Interface state density, D_{it}, as function of gate voltage extracted from the G_p/ω plots.

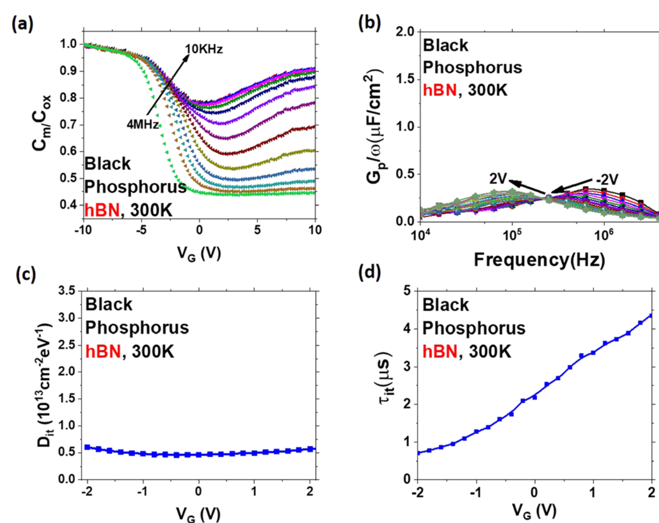

FIG. 4. CVs and interface states of a black phosphorus capacitor with hBN as gate dielectric at 300 K. (a) Capacitance as a function of gate voltage measured at various frequencies. (b) G_p/ω as a function of frequency at various gate voltages measured on black phosphorus capacitor with hBN as gate dielectrics, plotted in the same scale as Fig. 2(d) for comparison. (c) Extracted interface state density, D_{it}, as a function of temperature at various gate voltages for the black phosphorus capacitor with hBN as gate dielectric, plotted in the same scale as Fig. 2(f) for comparison. (d) Extracted interface-state time constant, τ_{it}, as a function of gate voltages.

We have systematically studied the capacitance and interface states of black phosphorus and WSe_2 capacitors with Al_2O_3 gate dielectrics. We found that the CVs in black phosphorus capacitors are ambipolar (symmetric about the minimum capacitance) and show low-frequency behavior even when the testing frequency is as high as 2.5 MHz, while the CVs in WSe_2 capacitors are unipolar (p-type) with high-frequency behavior even when the frequency is as low as 1 kHz. These dramatic differences in CV characteristics can be explained by the difference in bandgap sizes and doping concentrations in these two materials. The narrow bandgap of the black phosphorus flake (~0.3 eV) results in ample minority carriers at room temperature, which gives low-frequency CVs in black phosphorus capacitors, while the large bandgap (1.21 eV) of WSe_2 results in the high-frequency CVs. The natural p-type doping in WSe_2 leads to unipolar CVs while the very low doping in black phosphorus yields ambipolar CV characteristics. Although 2D materials are free of dangling bonds, the intimate contact of these 2D materials with high-k dielectrics can still generate a large number of interface traps. In this case, ALD Al_2O_3 is used as gate dielectric and the interface states can be as high as $10^{13}\,cm^{-2}eV^{-1}$. These interface states can significantly degrade the performance of electronic devices based on 2D materials. The interface state density in WSe_2 and black phosphorus shows strong voltage dependence. As the surface Fermi level shifts from midgap to the band edges, the interface-state density increases exponentially. In addition, the interface trap density in BP/Al_2O_3 capacitors is several times higher than that in the BP/BN capacitors. This work provides valuable information on the interface states of black phosphorus and WSe_2. These characterization and analysis methods can be broadly applied to other 2D semiconductors and serve as important tools for material selection, process optimization, and device design for 2D electronics and optoelectronics.

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