Mobility Measurement and Degradation Mechanisms of MOSFETs Made With Ultrathin High-k Dielectrics

Wenjuan Zhu, Jin-Ping Han, *Member, IEEE*, and T. P. Ma, *Fellow, IEEE*

***Abstract*—Accurate measurements and degradation mechanisms of the channel mobility for MOSFETs with HfO_2 as the gate dielectric have been systematically studied in this paper. The error in mobility extraction caused by a high density of interface traps for a MOSFET with high-k gate dielectric has been analyzed, and a new method to correct this error has been proposed. Other sources of error in mobility extraction, including channel resistance, gate leakage current, and contact resistance for a MOSFET with ultrathin high-k dielectric have also been investigated and reported in this paper. Based on the accurately measured channel mobility, we have analyzed the degradation mechanisms of channel mobility for a MOSFET with HfO_2 as the gate dielectric. The mobility degradation due to Coulomb scatting arising from interface trapped charges, and that due to remote soft optical phonon scattering are discussed.**

***Index Terms*—High-k dielectrics, mobility degradation, mobility measurement, MOSFETs.**

I. Introduction

To FULFILL the scaling scenario as projected in the International Technology Roadmap for Semiconductors (ITRS), it is widely believed that a high-k (high permittivity) dielectric is needed to replace SiO_2 as the CMOS gate dielectric to reduce significantly the gate leakage current [1]. After extensive research efforts by numerous groups, several high-k dielectrics have shown promising results [2]. However, there are still many challenges that have held back the actual implementation of these promising candidates. One of the major challenges is the significantly lower channel mobility for the transistors made of high-k gate dielectrics as compare to their SiO_2 counterparts [3], and there is not yet a clear understanding of the causes behind this degraded mobility. Besides the mobility degradation, the accuracy of the mobility measurement is also concern due to high density of interface traps and gate-leakage current. In this paper, we systemically studied the accurate measurement and the degradation mechanism of channel mobility for MOSFET with HfO_2 gate dielectrics.

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The effective mobility, $\mu_{\rm eff}$, can be obtained by measuring the drain current in the linear region [4]

$$\mu_{\rm eff} = \frac{L}{W} \cdot \frac{I_d(V_{\rm g})}{V_d Q_{\rm inv}(V_{\rm g})}. \tag{1}$$

In the past, many people used the following relationship to obtain $Q_{\rm inv}$ for a MOSFET with a relatively thick gate dielectric in strong inversion: $Q_{\rm inv} = C_{\rm ox}(V_{\rm g} - V_T)$.The fact that this is a poor approximation for MOSFETs with thin gate oxides began to be recognized in the early 1980s, and the split capacitance–voltage (*C–V*) technique was introduced [5] to extract $Q_{\rm inv}$ more accurately by measuring the gate-channel capacitance as a function of gate voltage

$$Q_{\rm inv} = \int_{-\infty}^{Vg} C_{\rm gc}(V_{\rm g}) dV_{\rm g}. \tag{2}$$

However, in this paper, we will show that this split *C–V* method to evaluate $Q_{\rm inv}$ is still very inadequate for high-k samples with high densities of interface traps and high leakage current.

The error introduced by the interface traps may arise from two sources: First, the interface traps can respond to the ac modulation signal in the capacitance measurement, which results in an additional parallel capacitance $C_{\rm it}$[6] that can result in an overcount of $Q_{\rm inv}$. This error can be minimized by using a higher frequency such that the interface traps cannot follow the ac signal [6], or corrected by subtracting out the effect of the interface traps if one can accurately measure the interface-trap density [7]. This aspect has been effectively dealt with by others [6], [7], and therefore is not the focus of this paper. Second, the interface traps can follow the dc voltage sweep, so that a change of $\delta V_{\rm g}$ in gate voltage not only results in a change of $\delta Q_{\rm inv}$ in the inversion charge, but also a change of $\delta Q_{\rm trap}$ in the charge trapped in interface traps [8], which can be expressed as $dV_{\rm g} = -(dQ_{\rm inv} + dQ_{\rm trap})/C_{\rm ox}$, where $C_{\rm ox}$ is the oxide capacitance per unit area. This *C–V* stretchout effect would result in an overestimated inversion charge [9]. In this paper, we propose a simple method to correct this error without having to measure the interface-trap density.

The effects of channel resistance in weak inversion, gate leakage current, and contact resistance on the mobility extraction are also presented in this paper, as they are distinctly different from the effects of interface traps.

Once we have obtained accurate values of the effective mobility, we will be in a position to investigate the possible mechanisms responsible for the mobility degradation in high-k gated MOSFETs, and some preliminary results that we have obtained will be presented.

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II. Experimental Details

Two kinds of device samples were used in this study: (1) nonself aligned n- and p-channel MOSFETs with Al as gate electrodes, and (2) selfaligned, poly-Si gated CMOS transistors with Hall-effect test structure. Their fabrication processes are briefly described below.

The nonself aligned MOSFETs are fabricated with ultrathin (EOT $\sim$ 2 nm) HfO_2 or HfAlO gate dielectrics on Si substrate with a dopant concentration of approximately $4 \times 10^{15}/\ \mathrm{cm}^3$. The source and drain regions of the n- and p- MOSFETs are implanted with phosphorous and BF_2 respectively, with an implantation dose of $5 \times 10^{15}/\mathrm{cm}^2$, and an implantation energy of 80 keV for both device types. After source/drain activation at 1000 °C, thin HfO_2 and HfAlO films are deposited by Jet-Vapor-deposition (JVD) [10]–[12] at room temperature on HF-last Si substrates. The post-deposition anneal (PDA) is done in forming gas. Aluminum is used as the gate electrode and source-drain contacts.

The self-aligned MOS Hall-effect structure and associated MOSFETs are fabricated using standard CMOS process with poly-Si gate, where HfO_2 gate dielectric was deposited by MOCVD on ultrathin (<1 nm) oxynitride [13]. Control samples with conventional SiO_2 as gate dielectric are also fabricated as references.

The uncorrected effective mobility is extracted from split *C–V* according to (1) and (2). The vertical effective electric field E_{eff} is determined from the equation: $E_{\mathrm{eff}} = (Q_D + \eta Q_{\mathrm{inv}}/\varepsilon_S)$, where η is a constant which has been reported to be 1/2 for electrons and 1/3 for holes [14], and Q_D is the depletion charge density extracted from accumulation *C–V*.

The Hall-effect mobility is measured as follows. After the channel is turned on by applying a gate voltage higher than the threshold voltage, a small voltage (100 mV) is applied to the drain (or source) to generate a small current along the channel. When a magnetic field, B ($\sim$0.37 T), is applied perpendicular to the Si surface, the Hall voltage, V_H, is measured between terminals R_s and L_s (or between R_D and L_D), where the positions of terminals R_s, L_s, R_D and L_D are illustrated in the inset of Fig. 2. In order to eliminate the error caused by various spurious voltages, the Hall voltages are measured at four combinations of magnetic fields and currents [15], and from which the average Hall voltage, V_{H-ave}, is calculated.

The Hall mobility, μ_H, is extracted according to the following equation [15]:

$$\mu_H = \frac{R_H}{\rho} = \frac{V_{H-ave}}{B \cdot I \cdot R \cdot \left(\frac{W}{L}\right)} \tag{3}$$

where R_H is the Hall coefficient, ρ is the resistivity, B is the magnetic field, I is the channel current, and R is the resistance between R_S and R_D (or L_S and L_D), W is the distance between R_S and L_S (or R_D and L_D), and L is the distance between R_S and R_D (or L_S and L_D) ($W/L = 4$ for the Hall structure used in this measurement). The relationship between the Hall mobility and the conductive mobility is given by $\mu_H = \gamma\mu_c$, where γ is the Hall scattering factor, which generally lies between 1 and 2 [16]. For most Hall-determined mobilities, γ is taken as unity [16], and is close to unity in our experiment, as to be shown below.

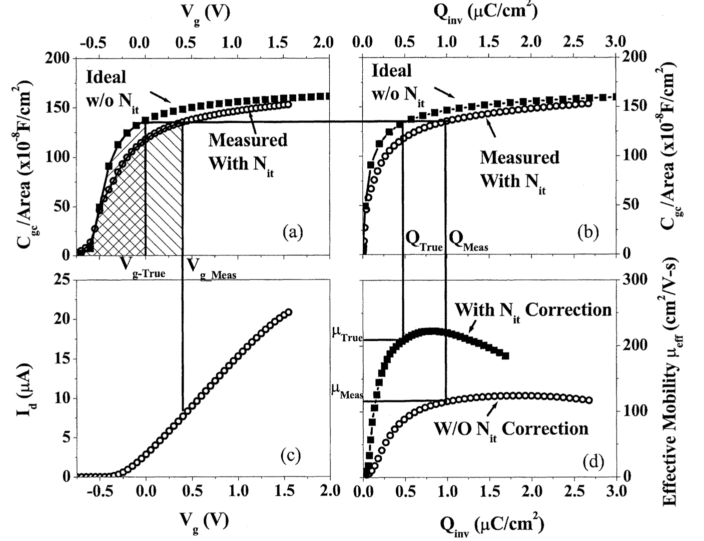

Fig. 1. Illustration of interface trap correction for extracting effective mobility. (a) Measured C_{gc} for MOSFETs with interface traps (open symbols) and ideal C_{gc} without interface traps (solid symbols); shadow areas result from the integration of the measured and ideal $C_{\mathrm{gc}} \sim V_{\mathrm{g}}$. (b) Surface charge in the inversion channel extracted from measured C_{gc} versus V_{g} curve (open symbols) and the one from ideal $C_{\mathrm{gc}} \sim V_{\mathrm{g}}$ curve (solid symbols). (c) $I_d \sim V_{\mathrm{g}}$ measured from the MOSFET with interface traps. (d) Uncorrected mobility calculated from the surface charge extracted from measured $C_{\mathrm{gc}} \sim V_{\mathrm{g}}$ (open symbol), and the corrected one obtained from the inversion charge extracted from ideal $C_{\mathrm{gc}} \sim V_{\mathrm{g}}$ (solid symbol).

III. Accurate Measurement of MOSFET With Ultrathin High-k Dielectrics

In this section, we will discuss the following factors that could result in significant errors in mobility extraction (1) carrier trapping, (2) channel resistance in weak inversion, (3) gate leakage current, and (4) contact resistance. Experimental results are given to illustrate the key points.

A. Carrier Trapping

Fig. 1 serves to illustrate this correction method. Fig. 1(a) shows the experimental high-frequency gate-channel capacitance C_{gc} (i.e., part of the split *C–V* data) of a HfO_2-gated nMOSFET with interface traps (including border traps [17]), along with the simulated ideal gate-channel capacitance without interface traps (for details of the simulation, see the Appendix). Assuming that traps in inversion for this sample cannot follow the high frequency ac signal, or the interface-trap capacitance, C_{it}, can be neglected for high-frequency measurement [6], then the gate-channel capacitance for metal gate samples is equal to [18]

$$C_{\mathrm{gc}} = \left(C_{\mathrm{ox}}^{-1} + C_{\mathrm{inv}}^{-1} + \frac{C_D}{C_{\mathrm{ox}}C_{\mathrm{inv}}}\right)^{-1} \tag{4}$$

(for poly-Si gate samples, see the Appendix), where C_{ox} is the oxide capacitance, C_{inv} is the inversion capacitance and C_D is the depletion capacitance. Here the inversion capacitance is defined as $C_{\mathrm{inv}} = (dQ_{\mathrm{inv}}/d\psi_s)$, where Q_{inv} is the inversion charge density, and ψ_s is the surface band bending in Si. Since the inversion capacitance C_{inv} is un-changed with or without traps, the gate-channel capacitance as a function of inversion charge, $C_{\mathrm{gc}}(Q_{\mathrm{inv}})$, should be the same with or without interface traps.

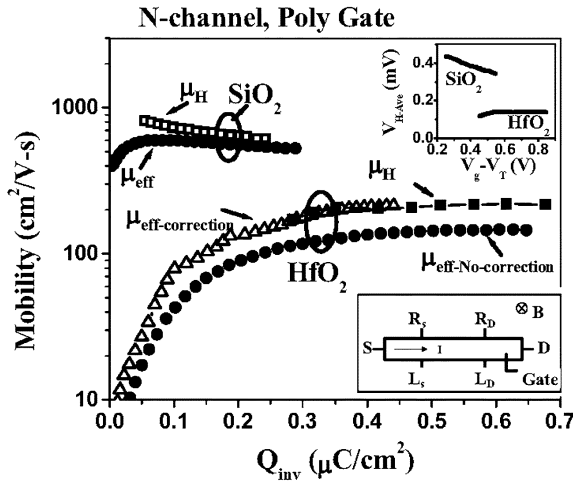

Fig. 2. Channel mobility data obtained from two split-*C–V* methods (both the conventional and the modified ones) and the Hall-effect method for a HfO_2 sample and a SiO_2 sample, plotted on a log scale. The EOT (equivalent oxide thickness) for the HfO_2 sample is ~ 2.25 nm and the thickness for the SiO_2 sample is ~ 3.45 nm. The substrate dopant concentration is about 1×10^{17} cm^{-3} for the HfO_2 sample and 6×10^{15} cm^{-3} for the SiO_2 sample. The lower inset shows the pad configuration of the MOS Hall-effect structure and the upper inset shows the average Hall voltage $V_{\rm H-Ave}$ as a function of $V_{\rm g} - V_T$ for SiO_2 and HfO_2.

However, the inversion charge density $Q_{\rm Meas}$ in Fig. 1(b), which we extracted by integrating the measured $C_{\rm gc-measured} \sim V_{\rm g}$ with interface traps, always exceeds $Q_{\rm True}$, which is obtained by integrating the ideal $C_{\rm gc-ideal} \sim V_{\rm g}$ curve for the same $C_{\rm gc}$. This is because $Q_{\rm Meas}$ contains both the inversion carrier charge and the interface trapped charge, while $Q_{\rm True}$ contains only the inversion carrier charge. Since only the mobile inversion channel charge $Q_{\rm True}$ contributes to the drain current, we should use $Q_{\rm True}$ rather than $Q_{\rm Meas}$ to calculate the mobility. Fig. 1(d) shows the mobilities $\mu_{\rm True}$ and $\mu_{\rm Meas}$ calculated from $Q_{\rm True}$ and $Q_{\rm Meas}$ respectively. As we can see, the corrected mobility $\mu_{\rm True}$ is much higher than the un-corrected mobility $\mu_{\rm Meas}$. Note that this correction is not affected by the existence of the oxide charge in the film, since the inversion charge density $Q_{\rm True}$, shown as the shaded area in Fig. 1(a), does not change when the curve is shifted along the $V_{\rm g}$ axis.

The validity of this correction method has been confirmed by Hall mobility measurement. Fig. 2 shows the channel mobility data obtained from both the split-*C–V* method and the Hall-effect method for an HfO_2 sample and a SiO_2 sample, plotted on a log scale. One can see that, for the SiO_2 sample, the mobility obtained from the Hall-effect method is very close to that from the split-*C–V* method, especially for $Q_{\rm inv} > 0.1\ {\rm C/cm^2}$. Since it is well known that the effective mobility extracted by the use of the split *C–V* method corresponds to the conductive mobility for a MOSFET sample with low interface-trap density ($<10^{11}$ cm^{-2}), we can estimate the scattering factor $\gamma = \mu_H/\mu_c$ to be about 1.1 at $Q_{\rm inv} = 0.2\ {\rm C/cm^2}$ for this MOSFET geometry, and the factor γ is approaching unity as the inversion charge density increases further, probably due to the carrier screening effect [19], [20] and/or the surface diffusion effect [19], [21]. For the inversion charge density $Q_{\rm inv} > 0.3\ {\rm C/cm^2}$, we should expect that the difference between the Hall mobility and conductive mobility to be well less than 10%. However, for the HfO_2 sample with $Q_{\rm inv} > 0.3\ {\rm C/cm^2}$, it is apparent that

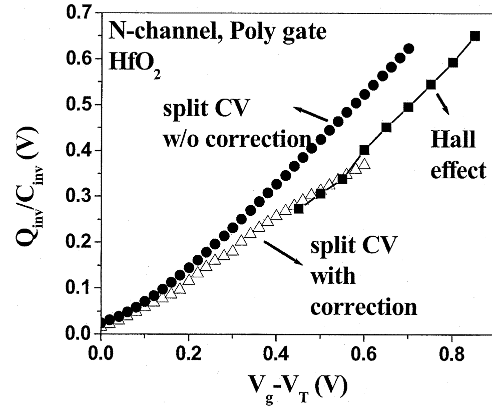

Fig. 3. Normalized inversion charge density as obtained from the Hall-effect method and split *C–V* with and without interface-trap correction.

the mobility obtained from the conventional split-*C–V* method is significantly lower than that obtained from the Hall-effect method (by about 40–50%), which we believe is due to the carrier trapping effect discussed in Section III above. By the use of our modified split-*C–V* method introduced in Section III above, however, we were able to correct the errors introduced in the conventional split-*C–V* method, and the corrected data are in excellent agreement with the Hall-effect mobility data.

To examine the magnitude of the carrier trapping effect, we plot in Fig. 3 the inversion layer charge density (normalized with respect to the inversion charge capacitance) as a function of gate voltage as measured by the three techniques discussed above. One can see that, compared to the data obtained from the Hall-effect method (which provides a direct measurement of the channel carrier density), the data obtained from the conventional split-*C–V* method indeed over-estimate the carrier density in the inversion layer, while the data from our modified split-*C–V* method nearly coincide with the Hall-effect data where both data sets exist. From the difference between the conventional split-*C–V* and the Hall-effect data, one can calculate the trap density, which in this case amounts to slightly over 1×10^{12} cm^{-2}, and this number is in good agreement with the trap density extracted from the subthreshold slope and charge trapping measurement [3], [22], [23].

It should be worth pointing out that $Q_{\rm Meas}$ is not simply equal to the sum of inversion charge $Q_{\rm inv}$ and the interface trapped charge $Q_{\rm it}$. In fact, it is less than that

$$Q_{\rm Meas} = Q_{\rm inv} + \int_0^{\rm Qit} \frac{C_{\rm gc}}{C_{\rm ox}} dQ_{\rm it} < Q_{\rm inv} + Q_{\rm it} \tag{5}$$

as derived in [24]. Therefore, there is an error if one simply subtracts the interface trapped charge $Q_{\rm it}$ from the measured surface charge $Q_{\rm Meas}$ to get the mobile inversion charge $Q_{\rm inv}$. On the other hand, since $Q_{\rm True} = \int_{-\infty}^{Vg1} C_{\rm gc-ideal} dV_{\rm g} = \int_{-\infty}^{Vg1} (dQ_{\rm inv}/dV_{\rm g}) dV_{\rm g} = Q_{\rm inv}$, one may reliably use $Q_{\rm True}$ to represent $Q_{\rm inv}$ in extracting the mobility.

To estimate the errors incurred by the trapping effect, we note that the error in the inversion charge extracted from split *C-V* without correction is

$$\Delta Q = Q_{\rm Meas} - Q_{\rm True} = \int_0^{Q_{\rm it}} \frac{C_{\rm gc}}{C_{\rm ox}} dQ_{\rm it}. \tag{6}$$

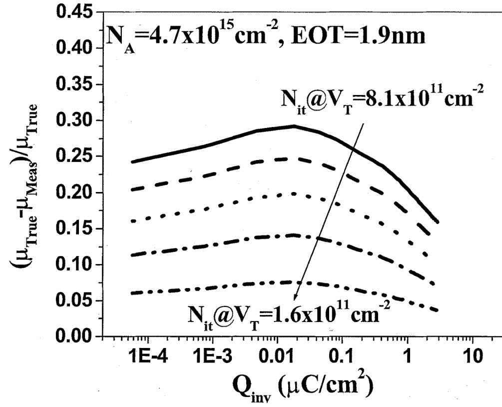

Fig. 4. Error percentage of mobility extracted from split *C–V* without interface-trap correction as a function of inversion charge for MOSFET with various interface-trap densities.

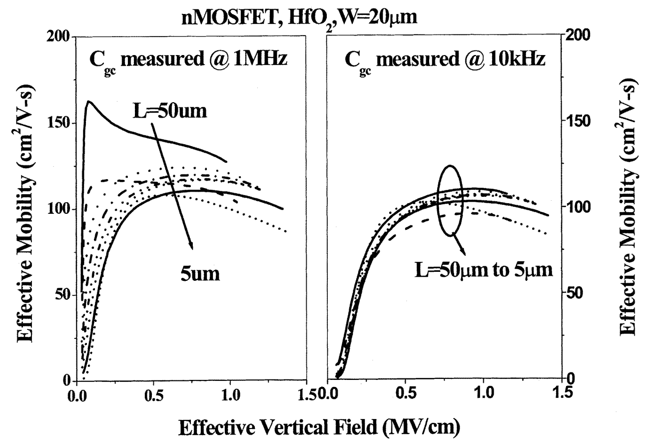

Fig. 5. Mobility values of HfO_2-gated NMOSFET with various channel lengths extracted from split *C–V* measured at (a) 1 MHz and (b) 10 KHz.

Correspondingly, the error in the mobility extracted from split *C–V* without correction is

$$\Delta\mu = \mu_{\rm Meas} - \mu_{\rm True} = \mu_{\rm True}\frac{-\Delta Q}{Q_{\rm inv} + \Delta Q}. \quad (7)$$

The error percentage of the mobility extracted from split *C–V* without correction is therefore

$$\frac{|\Delta\mu|}{\mu_{\rm True}} = \frac{|\mu_{\rm Meas} - \mu_{\rm True}|}{\mu_{\rm True}} = \frac{1}{1 + \frac{Q_{\rm inv}}{\Delta Q}}. \quad (8)$$

As we can see, the higher the interface-trap density, ΔQ, the larger the error percentage of the mobility extracted from split *C–V* without correction.

To get a rough idea as to the magnitude of the error percentage, let's assume an energy distribution of interface-trap density $D_{\rm it}$ $({\rm cm}^{-2}{\rm eV}^{-1})$ of the following form [7]

$$D_{\rm it} = \begin{cases} D_{\rm it}^0 \exp\left(\frac{E-E_c}{E_0}\right) & E < Ec \\ D_{\rm it}^0 & E \geq Ec \end{cases} \quad (9)$$

where $D_{\rm it}^0$ and E_0 are fitting parameters. The interface-trap density per unit area at certain energy level can be calculated according to the equation $N_{\rm it} = \int D_{\rm it} dE$.

The error in the inversion charge extracted from split *C–V* without correction can then be estimated according to (6), and the error percentage of the mobility extracted from split *C–V* without correction can be estimated according to (8). Fig. 4 shows the error percentage of the mobility extracted from split *C–V* without correction as a function of inversion charge for various interface-trap densities from 1.6×10^{11} ${\rm cm}^{-2}$ to 8.1×10^{11} ${\rm cm}^{-2}$ (assume $E_0 = 0.3$ eV, and $D_{\rm it}^0$ varies from 2×10^{12} ${\rm cm}^{-2}{\rm eV}^{-1}$ to 1×10^{13} ${\rm cm}^{-2}{\rm eV}^{-1}$). As we can see, the higher the interface-trap density is, the larger the error is. For the interface-trap density of 8.1×10^{11} ${\rm cm}^{-2}$, the error is as high as 30% at $Q_{\rm inv} = 0.02$ $\mu{\rm C}/{\rm cm}^2$. Note that, at low fields, the error increases with increasing field due to the increasing $C_{\rm gc}/C_{\rm ox}$ ratio, while at high fields, the error decreases with increasing field due to the increasing $Q_{\rm inv}/\Delta Q$ ratio.

Another thing worth noting is that, for highly doped substrate, the Fermi level is very near the minority bandedge when biased in inversion, and the time constants of the corresponding interface traps near the Fermi level are often sufficiently short to follow the high frequency ac signal. In such a case, the interface-trap capacitance $C_{\rm it}$ can no longer be neglected [7], and the measured gate-channel capacitance becomes $C_{\rm gc} = C_{\rm ox}(C_{\rm inv} + C_{\rm it})/(C_{\rm ox} + C_{\rm inv} + C_D + C_{\rm it})$.

To obtain the true inversion charge $Q_{\rm inv}$, one needs to correct for the interface-trap capacitance $C_{\rm it}$ according to the procedure presented in [7].

B. Channel Resistance in Weak Inversion

As we mentioned in Section I, in order to avoid the interference of the interface-trap capacitance $C_{\rm it}$, the frequency used in the split *C–V* measurement must be as high as practical [7]. In addition, for high-leakage films, in order to reduce the dissipation factor $(D = G/\omega C)$ and get an accurate inversion capacitance, one also needs to use the highest measurement frequency possible [25], [26]. However, this may cause a problem arising from channel resistance in weak inversion. Fig. 5(a) shows the apparent effective mobility of HfO_2-gated transistors with various gate lengths from 50 μm to 5 μm measured at 1 MHz. As one can see, there is significant channel length dependence of the extracted mobility, especially in the weak inversion region. This can be explained by the following relationship [27]

$$C_m = \frac{C}{(R_s G + 1)^2 + (\omega C R_s)^2} \quad (10)$$

where C_m is the measured capacitance in parallel mode, C is the actual capacitance, ω is the measurement frequency, R_s is the series resistance (including both channel resistance $R_{\rm ch}$ and contact resistance R_c, i.e., $R_s = R_{\rm ch} + R_c$). The equivalent circuit model of the MIS capacitor and the model for parallel capacitance measurement are illustrated in the upper inset of Fig. 6. In the weak inversion region, since the channel resistance $R_{\rm ch}$ is very large, the ω CR_s term may no longer be neglected, especially at a high frequency ω. This causes the measured capacitance to be smaller than the actual capacitance, giving rise to an underestimated inversion charge $Q_{\rm inv}$ and an overestimated mobility. This effect is more pronounced for devices with longer channels and at low fields, due to the larger channel resistance. In such a case, the measured gate-to-channel capacitance, $C_{\rm gc}$,

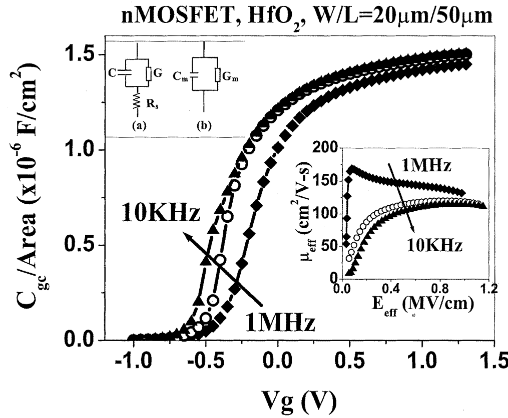

Fig. 6. Gate-to-channel capacitances of HfO_2-gated nMOSFET with $L = 50\ \mu m$ measured at three different frequencies. The upper inset shows (a) the equivalent circuit model of the MIS capacitor and (b) the model for parallel capacitance measurement. The lower inset shows the apparent mobility values of this device as extracted from this et of split-*C*–*V* curves.

becomes frequency dependent, as exemplified in Fig. 6, and the mobility extracted from the measured C_{gc} will also depend on the frequency, as shown in lower inset of Fig. 6, where one can see that the 1 MHz curve is artificially high at low fields, due to the large values of the term $\omega C R_s$. This error can be suppressed by using a lower frequency, as shown in Fig. 5(b), where the mobility extracted from a 10 kHz split-*C*–*V* curve displays much reduced channel length dependence as compared to the data in Fig. 5(a). Thus, the effects of interface traps and channel resistance determine the lower and higher limits of the measurement frequency, respectively.

C. Gate Leakage Current

For an ultrathin gate dielectric, the gate leakage current may affect the mobility extraction through the altered drain current. To obtain the corrected drain current, we measured I_d at two different V_ds ($V_{d1} = 20$ mV and $V_{d2} = 10$ mV). For a small V_d, the gate leakage current, I_{g}, is nearly unaffected by the small lateral field [28], and these two different V_ds should cause a similar amount of I_{g}. Therefore, the difference $[(I_d @ V_{d1}) - (I_d @ V_{d2})]$ is equivalent to the corrected I_d measured at $V_d = V_{d1} - V_{d2}$ [29]

$$I_{\mathrm{d-corrected}} = I_{d1} - I_{d2} = \frac{W}{L}\mu Q_{\mathrm{inv}}(V_{d1} - V_{d2}). \quad (11)$$

Using the corrected I_d, the corrected mobility is much higher than the one without correction at high fields, as shown in Fig. 7. Here we neglected the effect of the leakage current on the inversion capacitance measurement, due to the fact that the drain current rolloff is much more pronounced than the capacitance rolloff for this high-leakage film. It should be mentioned that a different method to correct the error caused by the leakage current has been reported recently [30].

D. Contact Resistance

The effect of contact resistance on mobility extraction is well known, and gets more important as the channel gets shorter. In the case when the contact resistance is not negligible compared to the channel resistance, the voltage across the channel

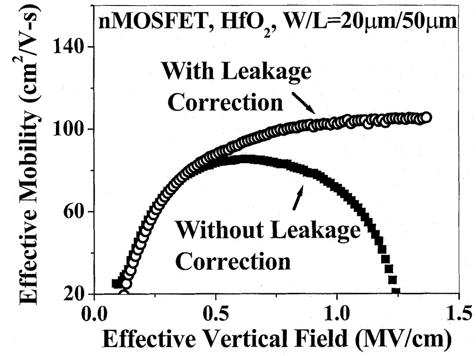

Fig. 7. Effective mobility of HfO_2-gated nMOSFET with and without gate leakage current correction.

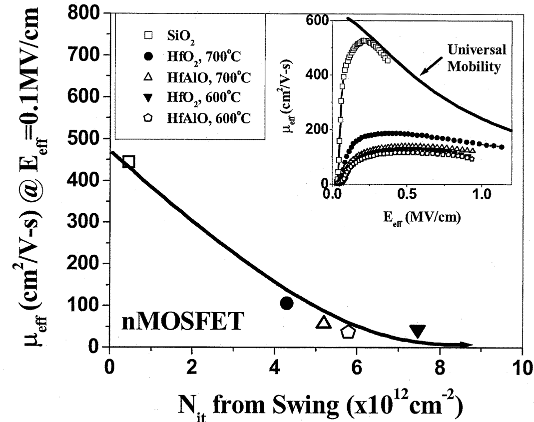

Fig. 8. Relationship between the effective mobility at $E_{\mathrm{eff}} = 0.1$ MV/cm and N_{it} extracted from subthreshold swing. The symbols are experimental results and line is for guiding the eye. The mobility data are taken from the inset, where it shows the effective mobility versus effective field, after interface-trap correction, for nMOSFETs with various gate dielectrics: SiO_2, HfO_2 (annealed at 600°C and 700 °C), and HfAlO (annealed at 600 °C and 700 °C).

becomes V_d–V_c, where V_c is the voltage across the contact. This can be corrected by measuring the contact resistance from appropriate test structures. The mobility with contact resistance correction is much higher than the uncorrected one, especially at high electric fields (data not shown).

IV. Mobility Degradation Mechanisms of HfO_2-Gated MOSFETs

Given the ability to measure the mobility accurately, we are now in a position to investigate the mobility degradation mechanisms for HfO_2-gated MOSFETs, with a particular focus on (1) Coulomb scattering due to interface traps, and (2) phonon scattering due to soft optical phonons [31].

A. Coulomb Scattering by Interface Traps

Fig. 8 shows the electron mobility as a function of N_{it}, after interface-trap correction, for nMOSFETs with various gate dielectrics: HfO_2 annealed at 600 °C and 700 °C, HfAlO annealed at 600 °C and 700 °C, and the SiO_2 control sample. The effective mobility data were taken at $E_{\mathrm{eff}} = 0.1$ MV/cm, and the N_{it} data were extracted from the subthreshold swings. It can be seen that the higher the interface-trap density, the lower the mobility. This indicates that coulomb scattering due to the interface

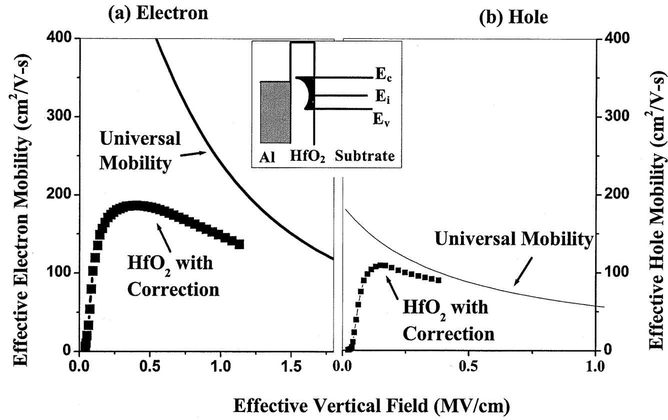

Fig. 9. Extracted (a) electron mobility and (b) hole mobility with interface-trap correction for HfO_2-gated MOSFETs annealed at 700 °C. The inset illustrates qualitatively the energy distribution of the interface traps.

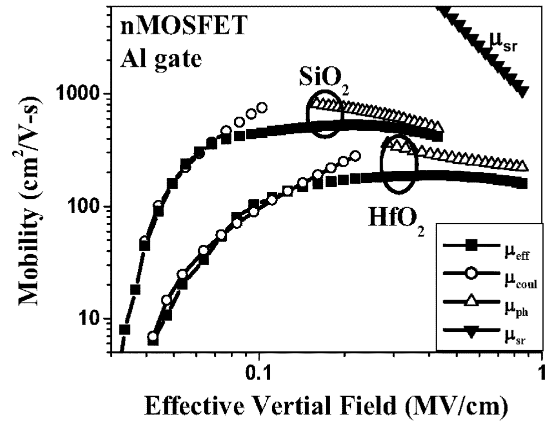

Fig. 10. Measured effective mobility, $\mu_{\rm eff}$, for HfO_2 sample and SiO_2 sample, along with their three components, including the component limited by Coulomb scattering, $\mu_{\rm coul}$, the component limited by surface roughness scattering, $\mu_{\rm sr}$, and the extracted mobility component limited by phonon scattering, $\mu_{\rm ph}$.

trapped charge is the dominant mechanism of mobility degradation for these high-k gated MOSFETs at low fields.

The energy distributions of the interface traps are found to be asymmetric in these samples, as shown in the inset of Fig. 9. The interface-trap density near the conduction band edge is higher than that near the valence band edge, as revealed by the larger subthreshold swing of the nMOSFET as compare to that of the pMOSFET (data not shown). Consequently, the degradation of hole mobility in pMOSFET is generally less severe than that for electron mobility in nMOSFET, as shown in Fig. 9. This is in agreement with that reported in [32].

B. Phonon Scattering

In addition to Coulomb scattering caused by high densities of interface traps and oxide charge, the scattering due to soft optical phonons in high-k dielectrics [31] is an intriguing possibility that cannot be overlooked, and we did look into this possibility.

To analyze the possible phonon scattering effect, we make use of the following equation, according to Matthiessens rule $1/\mu_{\rm ph} = 1/\mu_{\rm eff} - 1/\mu_{\rm coul} - 1/\mu_{\rm sr}$,where $\mu_{\rm eff}$ is the total effective mobility, $\mu_{\rm coul}$ is the mobility limited by Coulomb scattering, and $\mu_{\rm sr}$ is the mobility limited by surface roughness. To obtain the values for $\mu_{\rm ph}$, we extracted the values for $\mu_{\rm eff}$ from split *C–V* with interface-trap correction, those for $\mu_{\rm coul}$ from the effective mobility at low fields by linear fitting [33] and then extrapolated to high fields, and $\mu_{\rm sr}$ by using the equation $\mu_{\rm sr} = B \cdot E_{\rm eff}^{-2.6}$, where B is 4.5×10^{19}[14], assuming that the surface roughness for HfO_2 is similar to SiO_2. The unit for $E_{\rm eff}$ is V/m, and the unit for $\mu_{\rm sr}$ is $m^2/V - s$.

Fig. 10 shows the extracted mobility limited by phonon scattering for HfO_2-gated MOSFET and that for its SiO_2 counterpart. As we can see, the mobility limited by phonon scattering for the HfO_2-gated MOSFET is significantly lower than that for its SiO_2 counterpart, indicating a more severe phonon scattering for the former. Since the phonon scattering from the silicon substrate should be the same for both samples, this result suggests that the HfO_2-gated MOSFET has an additional source of phonon scattering, which is consistent with the high-k related soft optical phonon model proposed by Fischetti [31].

V. Conclusion

This paper discusses the accurate measurement and degradation mechanism of the channel mobility for MOSFETs with HfO_2 as the gate dielectric.

Four commonly encountered sources of error in mobility extraction for MOSFETs with ultrathin high-k dielectrics are addressed.

1) Trapping by high densities of interface traps (and/or border traps) could lead to a significant overecounting of the inversion charge and an underestimate of the channel mobility. This work proposes a simple and accurate method to correct this error by the use of a corrected split *C–V* curve without trapping effect. This method does not need additional measurement of the interface-trap density. The validity of this method has been confirmed by Hall-effect measuremnts of mobility and carrier concentration.
2) The high gate leakage current through the ultrathin high-k film could result in severe underestimation of the mobility at high fields, which can be corrected by taking the difference of drain currents measured at two different drain voltages.
3) The large channel resistance in weak inversion could result in artificially high mobility at low fields when measuring split *C–V* at high frequencies, which can be suppressed by using lower frequencies, provided that the frequency is not too low to pick up the effect of the interface-trap capacitance.
4) The error due to the contact resistance for short channel MOSFETs is well known, and can be corrected by subtracting the effect of the contact resistance measured from appropriate test structures.

Having been able to measure the mobility has allowed us to investigate the possible mechanisms responsible for the mobility degradation in HfO_2-gated MOSFET. Our preliminary results suggest that Coulomb scattering due to interface traps and oxide charge in HfO_2 is a major cause for mobility degradation, and there is evidence to support the notion that soft optical phonons in HfO_2 could also contribute to mobility degradation.

APPENDIX

For the device with poly-Si gate, the ideal gate-channel capacitance, $C_{\text{gc-poly}}$, and the low frequency gate-substrate capacitance, $C_{\text{LF-poly}}$, can be expressed as [35]

$$C_{\text{gc-poly}} = \left(C_{\text{poly}}^{-1} + C_{\text{ox}}^{-1} + C_{\text{inv}}^{-1} + \frac{C_D}{C_{\text{ox}} C_{\text{inv}}}\right)^{-1} \quad (12)$$

$$C_{\text{LF-poly}} = \left[C_{\text{poly}}^{-1} + C_{\text{ox}}^{-1} + (C_{inv} + C_D)^{-1}\right]^{-1} \quad (13)$$

where the oxide capacitance, C_{ox}, and depletion capacitance, C_D, are determined from the *C–V* curve measured in the accumulation and depletion regions, the poly depletion capacitance, C_{poly}, is determined from the low-frequency *C–V* curve at inversion region. $C_{\text{LF-poly}}$ can be simulated by the Hausers program [34] based on the above parameters. From (12) and (13), the relationship between $C_{\text{gc-poly}}$ and $C_{\text{LF-poly}}$ can be derived as

$$C_{\text{gc-poly}} = (C_{\text{LF-poly}}^{-1} - C_{\text{poly}}^{-1})^{-1} \times \left[1 - C_D(C_{LF-poly}^{-1} - C_{\text{poly}}^{-1} - C_{\text{ox}}^{-1})\right]. \quad (14)$$

From this equation, the ideal gate-channel capacitance for poly gate, $C_{\text{gc-poly}}$, can be calculated as a function of gate voltage.

For a device with metal gate, $C_{\text{poly}} = 0$ in (12)–(14).

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