Esaki Diodes Based on 2-D/3-D Heterojunctions

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***Abstract*— Esaki diodes based on interband tunneling have the characteristics of negative differential resistance (NDR) and ultrafast transient time, which lead to broad applications including oscillators, multivalue memories, and terahertz detectors. In this paper, we present the first demonstration of Esaki diodes based on 2-D/3-D heterojunctions—more specifically, chemical vapor deposition MoS_2 on degenerately doped silicon. As compared to traditional 3-D heterostructures, these 2-D/3-D heterostructures have the following advantages: dislocation-free 2-D crystals even when the lattices are mismatched, dangling bond-free surface, and capability for large-scale synthesis at low cost. In this paper, monolayer, bilayer, and trilayer MoS_2 are synthesized directly on degenerated Si substrate, forming the ultraclean heterostructures without surface contamination from tape and resist. Based on these pristine heterostructures, we are able to observe prominent NDR effect at room temperature. This NDR effect is attributed to the degenerately p-type doping in silicon and the natural n-type doping in MoS_2. We also found that the peak voltage corresponding to the local maximum tunneling current depends on the MoS_2 thickness. While MoS_2 is changing from the monolayer (0.7 nm) to bulk (9.5 nm), the peak voltage increases from 0.8 to 1.6 V. This phenomenon can be explained by the energy-level differences between the monolayer and bulk MoS_2. This paper provides the experimental groundwork for the synthesis of transition metal dichalcogenides on degenerately doped Si substrates and opens up new and exciting opportunities for electronic applications of 2-D/3-D heterostructures.**

***Index Terms*— 2-D/3-D heterojunctions, chemical vapor deposition (CVD), degenerately doped silicon, Esaki diodes, MoS_2.**

I. Introduction

ESAKI diodes have unique negative differential resistance (NDR) characteristics, which enable their applications in oscillators, terahertz detectors, multivalue memories, and analog-to-digital converters [1]–[3]. In addition, Esaki diodes serve as the critical components in tunneling field-effect transistors, which have potential applications in low-power electronics [4]–[6]. Various material stacks have been used in Esaki diodes, including Si, Ge, SiGe, group III-V, and their heterostructures [7]–[13]. Among these materials, III–V heterostructures grown by molecular-beam epitaxy produced the highest performing Esaki diodes [14]. The key factors that deteriorate the performance of III–V-based Esaki diodes are lattice mismatch (and associated dislocations), impurity scattering, polarization charges, and instability of space charge [14].

Recently, 2-D crystals have emerged as promising candidates for Esaki diodes [15], [16]. 2-D materials are free of surface dangling bonds, and 2-D heterostructures bonded by van der Waals forces are free of dislocations even when there is a large mismatch in lattice constants [17]. Esaki diodes based on $SnSE_2$/black phosphorus have been demonstrated, where the broken-gap band alignment between these two materials enables the NDR effect [15]. However, black phosphorus is not thermodynamically stable and is difficult to be synthesized in a large scale. In contrast, transition metal dichalcogenides (TMDs) can be synthesized in large scale via chemical vapor deposition (CVD) or molecular organic CVD [18]–[25]. However, most of the 2-D TMD heterostructures, such as MoS_2/WSE_2 heterostructure, do not have broken-gap band alignment. It is reported that by applying a vertical electric field to offset the band alignment between these two materials, NDR behavior can be observed [16]. However, the NDR effect in these devices is very weak and can only be observed at low temperatures. In addition, this device requires four electrodes instead of two electrodes in traditional Esaki diodes, which adds process complexity and device footprint.

In this paper, we propose a new type of Esaki diodes based on 2-D/3-D heterojunctions. In these devices, the 3-D material, such as silicon, is degenerately doped, while the 2-D material is naturally or intentionally doped into the opposite type to form a heterogeneous p-n-junction. This 2-D/3-D heterostructure can effectively eliminate the lattice-match restriction in a 3-D/3-D structure. As compared to the 2-D/2-D structure, the 2-D/3-D structure takes the advantages of the mature silicon technology and the commercially available degenerately doped silicon substrate. The 2-D TMDs can be grown directly on the silicon substrates, which will enable large-scale low-cost fabrication of the heterostructures and avoid surface/interface contamination from the transfer process. These pristine heterostructures enable us to observe prominent NDR effect at room temperature. This NDR effect is attributed to the energy-band alignments between the n-type

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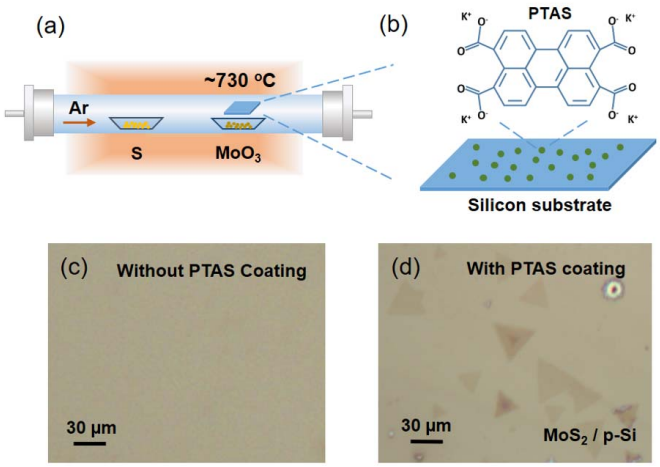

Fig. 1. Synthesis of MoS_2 on silicon substrates. (a) Schematic of the MoS_2 CVD system. (b) Chemical structure of PTAS. (c) and (d) Optical images of MoS_2 grown on degenerately doped silicon wafers without and with PTAS seeding promoter, respectively.

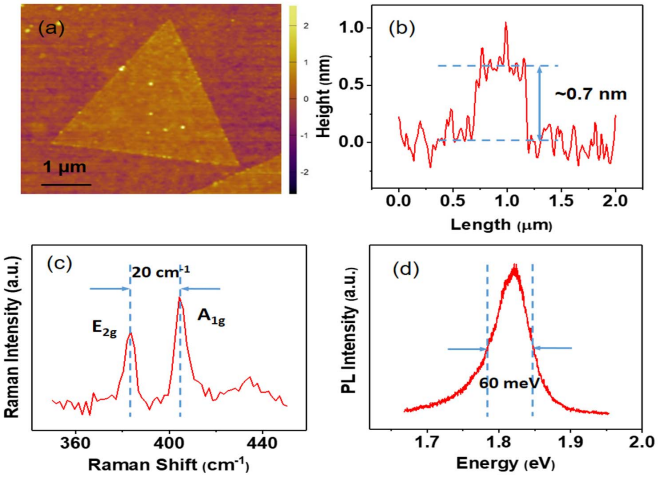

Fig. 2. Characterization of MoS_2 synthesized on silicon substrates. (a) and (b) AFM image and line profile of the MoS_2 film. (c) and (d) Raman and PL spectra of the MoS_2 synthesized by CVD, respectively.

MoS_2 and degenerately doped p-type Si. Moreover, the tunneling transports of MoS_2/p-Si heterostructures with different MoS_2 thicknesses are also investigated. We found that the peak voltage, V_P, is dependent on the MoS_2 thickness. As MoS_2 thickness changes from 0.7 nm (monolayer) to 9.5 nm, the peak voltage increases from 0.8 to 1.6 V, which can be explained by the thickness dependence of the energy bands in MoS_2.

II. Result and Discussion

Recently, considerable efforts have been made to grow monolayer MoS_2 nanosheets by using CVD [22], [26]. However, most of the work focuses on the synthesis of MoS_2 on SiO_2 or sapphire substrates. Here, we systematically investigated MoS_2 synthesis on degenerately doped silicon substrates with a resistivity of 0.001 Ωcm. Fig. 1(a) illustrates the setup of the CVD system. Molybdenum oxide (MoO_3) and sulfur (S) powders were used as precursors and were placed in two separated crucibles. The two zones with MoO_3 crucible and S crucibles were heated to 730 °C and 200 °C, respectively. The degenerately doped p-type Si substrates were facing down on the MoO_3 crucible. The MoS_2 layers were synthesized for 5 min with argon flow at ambient pressure. Without seeding promoter in the silicon substrate, the yield of MoS_2 was very low and only MoS_2 particles were obtained, as shown in Fig. 1(c). To address this nucleation issue, perylene-3,4,9, 10-tetracarboxylic acid tetrapotassium salt (PTAS) was used as the seeding promoter in the MoS_2 synthesis. Fig. 1(b) shows the molecular structure of PTAS. As compared to other aromatic molecules, PTAS has better thermal stability [18]. Moreover, the high solubility of PTAS in water can facilitate the uniform distribution of the seeds on the Si substrate. With PTAS as the seeding promoter, monolayer and multilayer MoS_2 nanosheets were successfully synthesized on a Si substrate, as shown in Fig. 1(d). Note that monolayer and multilayer MoS_2 coexist on the same wafer. Typically, multilayer MoS_2 is located at the center of the triangle, while monolayer MoS_2 is located at the outer zone of the triangle.

The grain size of synthesized MoS_2 is about 30 μm. The thickness of the MoS_2 is ~0.7 nm measured by atomic force microscopy (AFM) [Fig. 2(a) and (b)], indicating that it is a monolayer. Furthermore, the synthesized MoS_2 are characterized using Raman spectroscopy and photoluminescence (PL). In the Raman spectrum shown in Fig. 2(c), there are two peaks located at 384 and 404 cm^{-1}, corresponding to E_{2g} and A_{1g} modes in the monolayer MoS_2, respectively. It has been reported that the wavenumber difference between these two peaks (E_{2g} and A_{1g}) is about 20 cm^{-1} for monolayer MoS_2, whereas, it is 25 cm^{-1} for bulk MoS_2 [27]. The difference between these two peaks in our synthesized MoS_2 sample is ~20 cm^{-1}, further confirming that the synthesized MoS_2 film is a monolayer. The PL peak of the MoS_2 sample is at around 1.83 eV with a full-width at half-maximum intensity of 60 meV [Fig. 2(d)], corresponding to the feature of monolayer MoS_2 with high crystal quality [22]. In the future research, growth condition is to be further optimized to realize the wafer-scale growth of MoS_2 on the Si substrate.

Conductive AFM (C-AFM) measurements were performed to investigate the tunneling transport of our CVD MoS_2/Si heterostructures. As compared to the traditional IV measurement on vertical devices with electrodes, the C-AFM measurement has several advantages, including contamination free (avoiding the lithography-induced resist residuals), nanoscale probing on the local tunneling current (minimizing the noise induced by nonuniformity of the film), fast turn-around time, and direct correlation between the topography (layer thickness) and tunneling characteristics [28]. Fig. 3(a) shows the schematic of the C-AFM setup. Here, conductive Cr/Pt coated tips were used as the local electrical probes to obtain reliable measurements. The tip radius of our C-AFM is less than 25 nm. Note that for our C-AFM measurement, the current limit is set at 20 nA.

CVD monolayer, bilayer, and trilayer MoS_2 on silicon were identified by AFM in the topography mode, as shown in Fig. 3(b). The tunneling currents were measured *in situ* in the C-AFM mode as shown in Fig. 4(a). The zoomed-in

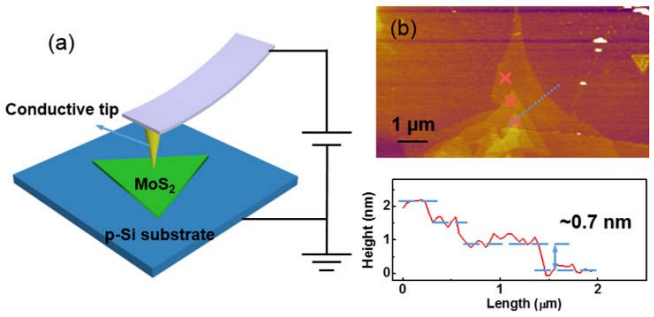

Fig. 3. (a) Schematic of the setup of C-AFM measurement. (b) AFM image and line profile of the CVD MoS_2 on a silicon substrate.

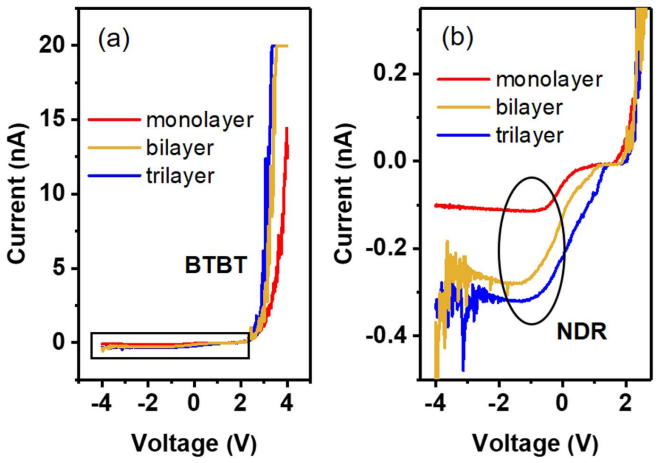

Fig. 4. C-AFM measurements of CVD MoS_2 on degenerately doped silicon. (a) Tunneling current as a function of voltage for monolayer, bilayer, and trilayer MoS2 grown on silicon substrate. (b) Zoomed-in view image of the IV curves in the negative bias region marked in the box on (a).

view of the negative bias regime is exhibited in Fig. 4(b). The IV curves show a nonlinear behavior. Since the voltage is applied on n-type MoS_2, the negatively applied voltage means a forward bias on the p-n-junction. We can see that NDR behavior appears in the forward bias region. For the monolayer MoS_2/Si heterostructure, the peak voltage (i.e., the voltage when the tunneling current reaches the local maximum), V_p, is ∼0.8 V. The peak-to-valley current ratio of the bilayer MoS_2/Si heterostructure is ∼1.16. This peak-to-valley current ratio is higher than that of MoS_2/WSE_2 heterostructure at room temperature but lower than that of $SnSE_2$/black phosphorus heterostructure [15], [16].

This NDR effect can be explained by the energy-band alignment between the degenerately doped silicon and naturally doped n-type MoS_2. Fig. 5(b)–(e) show the energy diagrams of MoS_2/p-Si heterostructure at various bias conditions and Fig. 5(a) illustrates the corresponding tunneling current at these bias conditions. When a reverse bias is applied on the heterostructure (i.e., a positive voltage is applied on the n-type MoS_2), the electrons from the valence band of Si tunnel into the conduction band of MoS_2 and the tunneling current increases exponentially with increasing reverse bias [Fig. 5(b)]. The corresponding current is designated by a

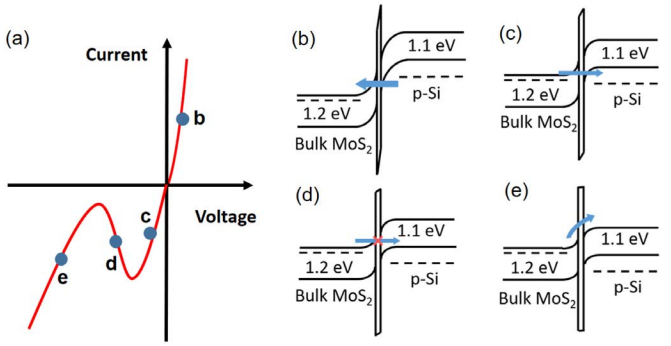

Fig. 5. Energy diagrams of MoS_2/Si heterojunctions at various bias conditions. (a) Illustration of the IV curves with NDR effect. Four different regions are marked as b–e. The corresponding energy diagrams are illustrated in (b) reverse bias, (c) small forward bias with band-to-band tunneling current flowing, (d) forward bias such that the tunneling current is prohibited, and (e) high forward bias with thermal current flowing.

circle "b" on the IV curve [Fig. 5(a)]. When a small forward bias is applied, a band of energies exists for which there are filled states on the n-type MoS_2 side, while unoccupied states on the p-type Si, thus the electrons can tunnel from n-MoS_2 to p-Si [Fig. 5(c)]. When the forward bias is further increased, there are fewer unoccupied available states on the p-Si side, which allows the tunneling of electrons from the n-MoS_2 side. When the decrement of the tunneling current due to reduced available states is dominant over the increment of the tunneling current due to an increased electric field across the junction, the tunneling current starts to decrease. As the forward bias is further increased such that the conduction band edge of the n-type MoS_2 matches or exceeds the valence band edge of the p-type Si, electrons in MoS_2 can no longer tunnel into a valence band state in silicon [Fig. 5(d)]. With still further increase in the bias, the electron and hole diffusion barrier will reduce and the thermal current will start to increase, therefore, the total current will increase again [Fig. 5(e)]. The decreasing portion of the tunneling current after the peak current [region d in Fig. 5(a)] gives rise to the NDR effect. Note that typically 2-D MoS_2 grown by the CVD method is naturally n-type doped [19], [20]. To create Esaki diodes, degenerately doped p-type Si substrates were used. At equilibrium, if the conduction band edge of MoS_2 in the neutral region is lower than the valence band edge of silicon in the neutral region, NDR effect can occur. Here, we assume that there is a thin layer of native silicon oxide at the interface between MoS_2 and silicon. It is reported that the thickness of the native oxide on a silicon wafer is typically ∼1 nm at room temperature [29]. The traps in the native silicon oxide layer and the dangling bonds of the silicon surface can result in trap-assisted tunneling and degrade the peak-to-valley ratio.

To further investigate the thickness-dependent tunneling transport of MoS_2/Si heterostructures, thicker MoS_2 nanosheets are mechanically exfoliated on degenerately doped p-type Si substrate. The thickness ranges from 1.8 to 9.5 nm as confirmed by AFM, as shown in Fig. 6(a). Then, the local IV curves are measured by C-AFM with the bias from 4 to −4 V, as shown in Fig. 6(b). The zoomed-in view of the negative bias

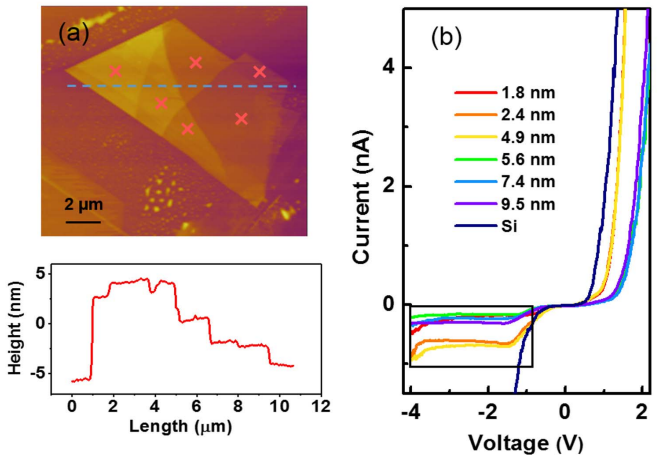

Fig. 6. C-AFM measurements of exfoliated MoS_2 on a degenerately doped p-type silicon substrate. (a) AFM image and line profile of the MoS_2 on silicon. (b) Tunneling current as a function of applied voltage for MoS_2 with various thicknesses.

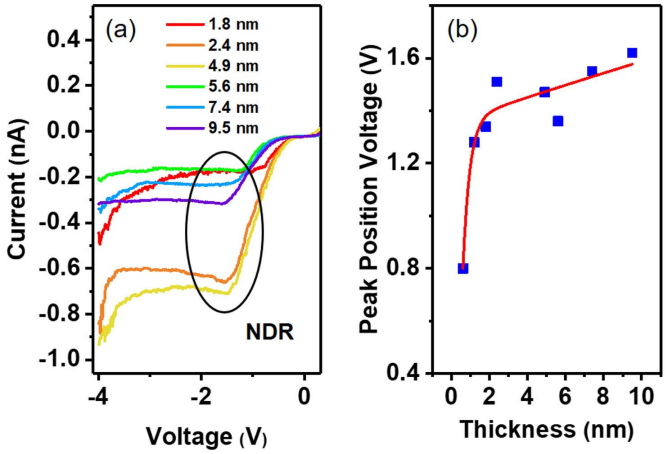

Fig. 7. Thickness dependence of the peak voltage. (a) Zoomed-in view of the tunneling current as a function of applied voltage in the negative bias regime for MoS_2 with various thickness. (b) Peak voltage as a function of MoS_2 thickness. Blue squares: measured data. Red line: guiding eyes only.

regime is shown in Fig. 7(a). Importantly, the NDR behaviors are clearly observed in MoS_2/Si heterostructures with various MoS_2 thicknesses. In contrast, there is no NDR effect observed in the bare Si sample without MoS_2. This indicates that the NDR effect observed in MoS_2/Si samples is related to the MoS_2 layer. Furthermore, we found that the peak voltages are dependent on the MoS_2 thickness. As shown in Fig. 7(b), as the MoS_2 thickness increases from 0.7 nm (monolayer) to 9.5 nm (bulk), the peak voltage increases from 0.8 to 1.6 V. This can be explained by the energy-level differences between the monolayer and bulk MoS_2. The peak-to-valley ratios for different MoS_2 thicknesses range from 1.2 to 1.05, with no strong dependence on the film thickness. The IV curves show nonzero current at zero voltage, which results from the background noise current at tens of picoampere.

Fig. 8(a) shows the energy diagram of the isolated monolayer MoS_2, bulk MoS_2, and degenerately doped p-type

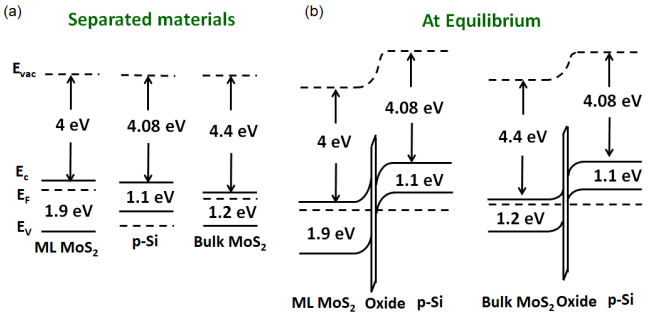

Fig. 8. Energy diagrams of MoS_2/Si heterojunctions. (a) Energy diagram of isolated monolayer MoS_2, bulk MoS_2, and degenerately doped silicon before they contact each other. (b) Energy diagrams of monolayer-MoS_2/Si and bulk-MoS_2/Si heterostructures.

silicon. Fig. 8(b) shows the energy diagram of monolayer-MoS_2/Si and bulk-MoS_2/Si heterostructures. Based on the theoretical calculations, the electron affinity of MoS_2 is 4 eV for monolayer and 4.4 eV for bulk. Experimentally, it is reported that the work function of bilayer MoS_2 is about 0.15 eV lower than that of six-layer MoS_2 [30]. As the thickness of MoS_2 increases from a monolayer to bulk, if the work function increment is less than the electron affinity increment, then the energy difference between the conduction band edge and the Fermi level in the MoS_2 neutral region, $E_{c-\mathrm{MoS2}} - E_F$, will decrease. This decrease means that the energy difference between the valence band edge in Si and the conduction band edge in MoS_2 in the neutral region, $E_{v-\mathrm{Si}} - E_{c-\mathrm{MoS2}}$, will increase, leading to an increase in the peak voltage as the thickness of MoS_2 increases. Note that in these measurements, the true voltage dropped on the heterojunction is less than the applied voltage, due to the voltage consumed on the tip/MoS_2 contact, MoS_2 neutral region, interfacial oxide layer, and/or the air gap between the tip and the sample.

III. Conclusion

In summary, we have first demonstrated Esaki diodes based on 2-D/3-D heterojunctions: CVD MoS_2 on degenerately doped silicon substrates, with prominent NDR effect at room temperature. Monolayer MoS_2 nanosheets are successfully synthesized on the degenerately doped p-Si substrate directly by CVD using PTAS as the seeding promoter. AFM, Raman, and PL characterizations confirmed that the synthesized MoS_2 is a monolayer with high crystal quality. Furthermore, C-AFM is carried out to investigate the tunneling transport of MoS_2/Si heterostructures. The NDR effect is observed in the forward bias regime, which can be explained by the band alignment between MoS_2 and degenerately doped Si. We also found that the peak voltage is dependent on the MoS_2 thickness. When the MoS_2 thickness increases from 0.7 to 9.5 nm, the peak voltage increases from 0.8 to 1.6 V. This phenomenon is attributed to the difference in the energy levels in the monolayer and bulk MoS_2. This paper will provide a new path for Esaki diodes based on synthesized 2-D/3-D heterostructures. This new type of the device has the advantages of high performance and large-scale manufacturability with low cost, giving it broad applications in electronics and optoelectronics.

REFERENCES

[1] J. P. Sun, G. I. Haddad, P. Mazumder, and J. N. Schulman, "Resonant tunneling diodes: Models and properties," *Proc. IEEE*, vol. 86, no. 4, pp. 641–661, Apr. 1998.

[2] J. Esch, "Prolog to resonant tunneling diodes: Models and properties," *Proc. IEEE*, vol. 86, no. 4, pp. 639–640, Apr. 1998.

[3] S. Takahagi, H. Shin-Ya, K. Asakawa, M. Saito, and M. Suhara, "Equivalent circuit model of triple-barrier resonant tunneling diodes monolithically integrated with bow-tie antennas and analysis of rectification properties towards ultra wideband terahertz detections," *Jpn. J. Appl. Phys.*, vol. 50, no. 1, p. 01BG01, Jan. 2011.

[4] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007, doi: 10.1109/LED.2007.901273.

[5] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[6] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196805, Nov. 2004.

[7] W. Y. Fung, L. Chen, and W. Lu, "Esaki tunnel diodes based on vertical Si-Ge nanowire heterojunctions," *Appl. Phys. Lett.*, vol. 99, no. 9, p. 092108, Aug. 2011.

[8] K. Majumdar *et al.*, "Mapping defect density in MBE grown $In_{0.53}Ga_{0.47}As$ epitaxial layers on Si substrate using Esaki diode valley characteristics," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2049–2055, Jun. 2014.

[9] M. Oehme *et al.*, "Si Esaki diodes with high peak to valley current ratios," *Appl. Phys. Lett.*, vol. 95, no. 24, p. 242109, Dec. 2009.

[10] D. Pawlik *et al.*, " Benchmarking and improving III-V Esaki diode performance with a record 2.2 MA/cm^2 peak current density to enhance TFET drive current," in *IEDM Tech. Dig.*, Dec. 2012, pp. 27.1.1–27.1.3.

[11] P. Thomas *et al.*, "Performance evaluation of $In_{0.53}Ga_{0.47}As$ Esaki tunnel diodes on silicon and InP substrates," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2450–2456, Aug. 2015.

[12] L.-E. Wernersson *et al.*, "A combined chemical vapor deposition and rapid thermal diffusion process for SiGe Esaki diodes by ultra-shallow junction formation," *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 594–598, Sep. 2005.

[13] K. Zhu, W. Wang, Q. Shao, D. Zhao, Y. Lu, and N. Ianno, "Self-assembled ordered arrays of nanoscale germanium Esaki tunnel diodes," *Appl. Phys. Lett.*, vol. 98, no. 17, p. 173110, Apr. 2011.

[14] C. Bayram, Z. Vashaei, and M. Razeghi, "AlN/GaN double-barrier resonant tunneling diodes grown by metal-organic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 96, no. 4, p. 042103, Jan. 2010.

[15] R. Yan *et al.*, "Esaki diodes in van der Waals heterojunctions with broken-gap energy band alignment," *Nano Lett.*, vol. 15, no. 9, pp. 5791–5798, Sep. 2015.

[16] T. Roy *et al.*, "Dual-gated MoS_2/WSe_2 van der Waals tunnel diodes and transistors," *ACS Nano*, vol. 9, no. 2, pp. 2071–2079, Feb. 2015.

[17] A. K. Geim and I. V. Grigorieva, "Van der Waals heterostructures," *Nature*, vol. 499, no. 7459, pp. 419–425, 2013.

[18] Y.-H. Lee *et al.*, "Synthesis and transfer of single-layer transition metal disulfides on diverse surfaces," *Nano Lett.*, vol. 13, no. 4, pp. 1852–1857, 2013.

[19] S. Wu, C. Huang, G. Aivazian, J. S. Ross, D. H. Cobden, and X. D. Xu, "Vapor–solid growth of high optical quality MoS_2 monolayers with near-unity valley polarization," *ACS Nano*, vol. 7, no. 3, pp. 2768–2772, Mar. 2013.

[20] L. Chen *et al.*, "Screw-dislocation-driven growth of two-dimensional few-layer and pyramid-like WSe_2 by sulfur-assisted chemical vapor deposition," *ACS Nano*, vol. 8, no. 11, pp. 11543–11551, Nov. 2014.

[21] S. Najmaei *et al.*, "Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers," *Nature Mater.*, vol. 12, no. 8, pp. 754–759, 2013.

[22] A. M. van der Zande *et al.*, "Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide," *Nature Mater.*, vol. 12, no. 6, pp. 554–561, Jun. 2013.

[23] H. Zhou *et al.*, "Large area growth and electrical properties of p-type WSe_2 atomic layers," *Nano Lett.*, vol. 15, no. 1, pp. 709–713, Jan. 2015.

[24] K. Kang *et al.*, "High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity," *Nature*, vol. 520, no. 7549, pp. 656–660, 2015.

[25] G. R. Bhimanapati *et al.*, "Recent advances in two-dimensional materials beyond graphene," *ACS Nano*, vol. 9, no. 12, pp. 11509–11539, Nov. 2015, doi: 10.1021/acsnano.5b05556.

[26] K.-K. Liu *et al.*, "Growth of large-area and highly crystalline MoS_2 thin layers on insulating substrates," *Nano Lett.*, vol. 12, no. 3, pp. 1538–1544, Mar. 2012.

[27] A. Molina-Sánchez and L. Wirtz, "Phonons in single-layer and few-layer MoS_2 and WS_2," *Phys. Rev. B, Condens. Matter*, vol. 84, no. 15, p. 155413, Oct. 2011.

[28] T. Van Nguyen, M. V. Nguyen, G. Lin, N. Rao, X. Xie, and D.-M. Zhu, "Characterization of surface ionic activity of proton conductive membranes by conductive atomic force microscopy," *Electrochem. Solid State Lett.*, vol. 9, no. 2, pp. A88–A91, 2006.

[29] R. Doering and Y. Nishi, *Handbook of Semiconductor Manufacturing Technology*, 2nd ed. Boca Raton, FL, USA: CRC Press, 2008.

[30] S. Choi, Z. Shaolin, and W. Yang, "Layer-number-dependent work function of MoS_2 nanoflakes," *J. Korean Phys. Soc.*, vol. 64, no. 10, pp. 1550–1555, May 2014.

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