

Synthesis and Electrical Characterization of Monolayer Tungsten Diselenide

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Abstract: In this paper, we systematically investigated the synthesis of the monolayer tungsten diselenide (WSe_2) by chemical vapor deposition (CVD) and studied the current transport of monolayer WSe_2 . We found that the hydrogen flow rate and the amount of WO_3 precursor play an important role in the morphology of the WSe_2 . The hole mobility of the monolayer WSe_2 grown by CVD can reach $40 \text{ cm}^2/\text{V}\cdot\text{s}$ at carrier density of $2.7 \times 10^{12} \text{ cm}^{-2}$. At low temperatures, the carrier mobility increases with higher temperature due to Coulomb scattering. When the temperature is above 250 K, the mobility decreases with increasing temperature due to phonon scattering. The interface trap density of the back-gated WSe_2 transistors is extracted from the subthreshold swing at various temperatures. The interface trap density increases monotonically when the energy level approaches the valence band edge.

Introduction: WSe_2 is an important member of the transition metal dichalcogenide (TMDC) family due to its smaller effective electron and hole masses if compared to most of the other TMDCs, and more importantly due to its ambipolar characteristics.^{1,2} The small effective mass implies high carrier mobilities, while the ambipolar conduction is essential for complementary metal oxide semiconductor (CMOS) circuits.³⁻⁵ In this paper, we investigated the growth of monolayer WSe_2 by CVD and studied the current transport of monolayer WSe_2 .

Results and Discussion: Solid precursor WO_3 and Se power were used to synthesize WSe_2 on Si/SiO_2 substrate in a CVD chamber. Various growth conditions have been investigated, including hydrogen flow rate, WO_3 precursor amount, growth temperature, and argon flow rate. We found that these growth parameters can significantly influence the morphology of the WSe_2 . With systematic optimization of the growth condition, high-quality monolayer WSe_2 was obtained. Figure 1a and 1b show the typical optical image and photoluminescence (PL) spectrum of the synthesized WSe_2 . Bright light emission at $\sim 1.60 \text{ eV}$ and symmetric single PL peak suggest the direct band gap nature of monolayer WSe_2 , showing good agreement with other recent reports about PL of monolayer WSe_2 .⁶ The Raman and AFM measurement also confirmed its monolayer character. The carrier mobility of the CVD WSe_2 is studied in the long channel transistors using the four-point method. Figure 2a shows the conductance as a function of gate voltage measured at various temperatures. The extracted field effect mobility as a function of temperature is shown in Fig. 2b. At low temperatures, the mobility increases with increasing temperature. When the temperature is above 250 K, the mobility decreases with increasing temperature. At low temperatures, Coulomb scattering dominants, while at high temperatures, phonon scattering plays an important role. The mobility of monolayer WSe_2 can reach $40 \text{ cm}^2/\text{V}\cdot\text{s}$, at a carrier density of $2.7 \times 10^{12} \text{ cm}^{-2}$. This high carrier mobility indicates the good quality of the monolayer WSe_2 synthesized using the optimized condition. The interface trap density of the CVD WSe_2 is evaluated by measuring the subthreshold swing at various temperatures on the long channel transistors. Figure 3a shows the measured subthreshold swing as a function of gate voltage. The interface trap density, D_{it} , is extracted from the subthreshold swing and plotted as a function of gate overdrive, $V_G - V_T$, at various temperatures, shown in Fig. 3b. As the gate overdrive, $V_G - V_T$, decreases, i.e. as the Fermi level at the $\text{WSe}_2/\text{oxide}$ interface is approaching the valence band edge, the interface trap density increases, which is similar to the energy distribution of the interface traps in silicon.

Summary: We have systematically investigated the synthesis of monolayer WSe_2 using CVD and studied the electric transport of CVD WSe_2 . We found that the optimized growth conditions can result in large grain WSe_2 with high mobility (up to $40 \text{ cm}^2/\text{V}\cdot\text{s}$). The mobility of the CVD WSe_2 increases with increasing temperature at low temperatures due to Coulomb scattering, while reduces with increasing temperature when the temperature is above 250 K due to phonon scattering. The interface trap density of WSe_2 was extracted from the subthreshold swings. The interface trap density of CVD WSe_2 increases as the energy level is approaching the valence band edge. These findings will enrich the knowledge of the electric transport in CVD WSe_2 and the scaled electronic devices based on monolayer TMDCs.

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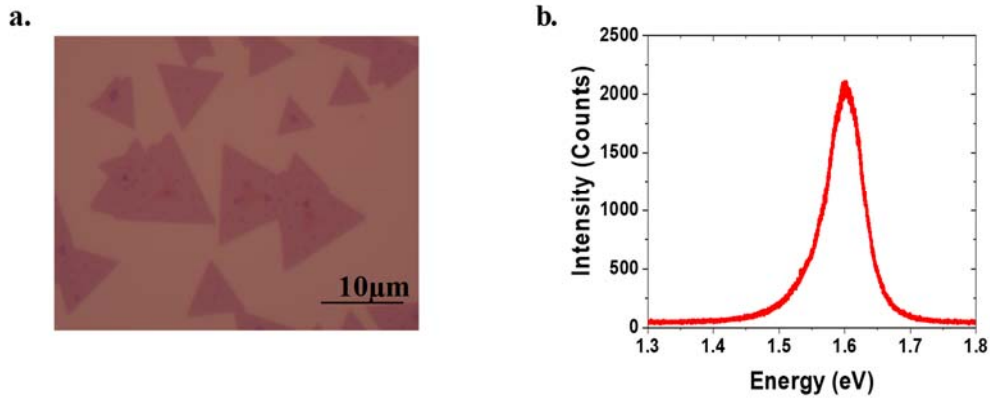


Figure 1. (a) Optical image, and (b) photoluminescence spectrum of monolayer WSe₂ grown by CVD.

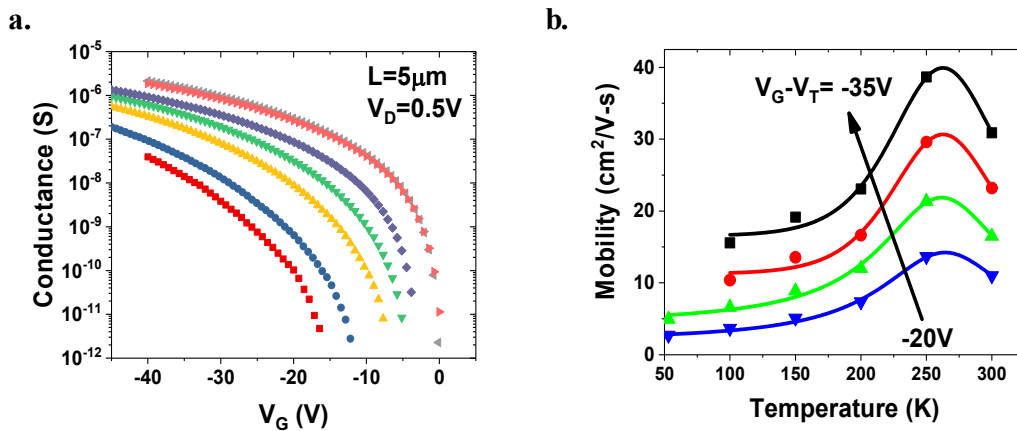


Figure 2 (a) Conductance of the back-gated WSe₂ transistors measured at various temperatures. (b) Extracted hole mobility as a function of temperature at various gate overdrive.

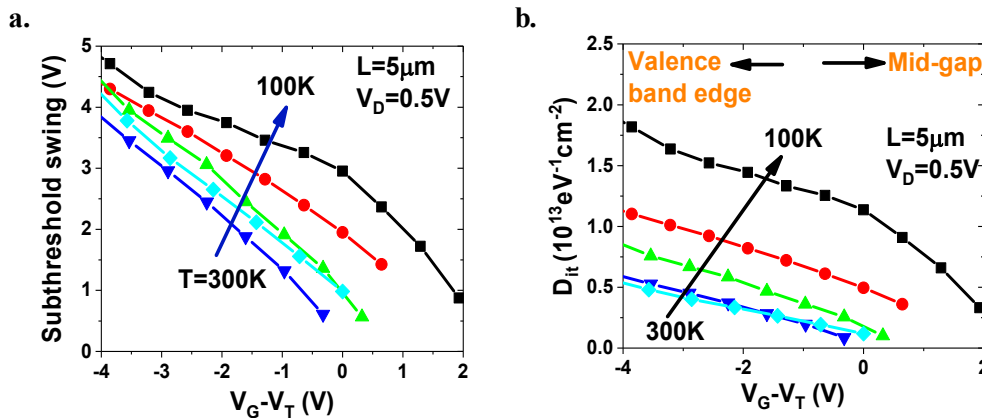


Figure 3. Interface states in back-gated WSe₂ transistors. (a) Subthreshold swing as a function of gate overdrive, $V_G - V_T$, at various temperatures. (c) Extracted interface trap density as a function of gate overdrive.

Reference:

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